

Model Name: GA-B85M-D3H

SHEET TITLE Revision 1.1

01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	CPU_LGA1150-A
05	CPU_LGA1150-B
06	CPU_LGA1150-C
07	DDR III CHANNEL A 1,2
08	DDR III CHANNEL B 1,2
09	PCH_FDI,DMI,USB,PCIE,NVRAM
10	PCH_DP,CLK BUFFER
11	PCH_HOST,SATA,PCI
12	PCH_GPIO,CTRL,AUDIO
13	PCH_PWR,GND
14	PCI EXPRESS*16 SLOT
15	PCI EXPRESS*4 SLOT
16	PCI SLOT1,2
17	ITE 8728 LPC IO
18	COM,KB_MS_USB,USB30_20
19	HWM,FAN CTRL,OV,-PROCHOT
20	DUAL BIOS
21	FP,FUSB,SPK,SATALED
22	Realtek ALC892-GR
23	REAR AUDIO JACK
24	REALTEK RTL8111F
25	DISCRETE POWER
26	ATX , CLOCK GEN, TPM
27	VCORE ISL95820_1

SHEET TITLE

28	VCORE ISL95820_2
29	RT8120_DDR POWER
30	LPT, M3 POWER
31	DVI, HDMI
32	IT8892E

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Gigabyte Technology		
Title		
Cover Sheet		
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Model Name: GA-B85M-D3H

Component value change history

Revision 1.1
P-Code U12090-0

[illegible]

Circuit or PCB layout change

[illegible]

BLOCK DIAGRAM

PCI EXPRESS X16

DVI, HDMI

RGB

PCI EXPRESS X4

PCI BRIDGE ITE IT8892

Realtek RTL8111F

USB2.0 PORTS X12

USB3.0 PORTS X4

INTEL LGA1150

VRD12.5

CHANNEL A
DDRIII DIMM X 2

CHANNEL B
DDRIII DIMM X 2

PCH (B85)

SATAIII*4/SATAII*2

DUAL BIOS

LPC I/O ITE8728

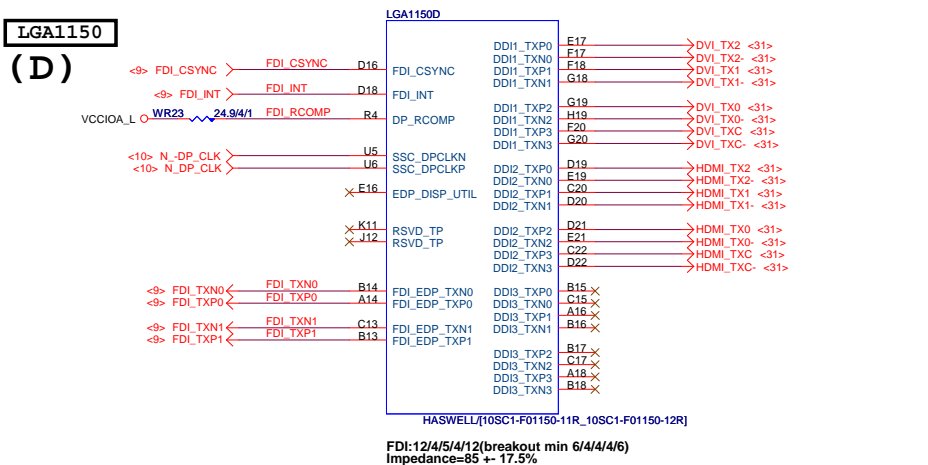
I/O PORTS :
COM KB/MS

FRONT PANEL / FAN

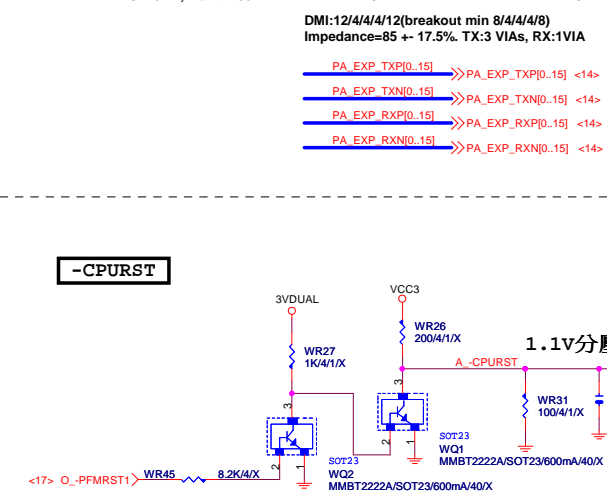
Realtek ALC892

AUDIO PORTS :
FRONT AUDIO
LIN_OUT LINE_IN MIC CD_IN
SURROUND CEN/LEF SURR BACK

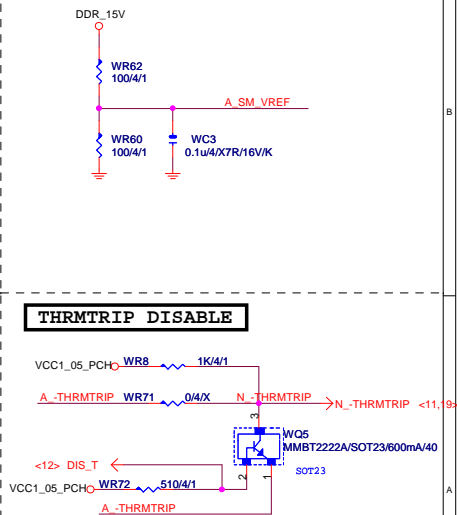
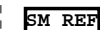
LGA1150
(D)



-CPURST



CPU PU/PD



THRMTRIP DISABLE

LG A1150A

HASWELL/10SC1-F01150-11R_10SC1-F01150-12R]

LGA1150B

<8> VREF_DQB \



CR



```

MODT_A[0..3]

```

```

<7> MODT_A[0..3] <=> MODT_B[0..3]
<8> MODT_B[0..3] <=> MODT_A[0..3]

<7> MDA[0..63] <=> MDBA[0..63]
<8> MDBA[0..63] <=> MDA[0..63]

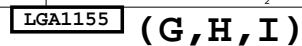
<7> DQSA[0..7] <=> DQSB[0..7]
<7> -DQSA[0..7] <=> -DQSB[0..7]

<7> MAAA[0..15] <=> MAAA[0..15]
<8> MAAB[0..15] <=> MAAB[0..15]

<8> DQSB[0..7] <=> DQSA[0..7]
<8> -DQSB[0..7] <=> -DQSA[0..7]

```

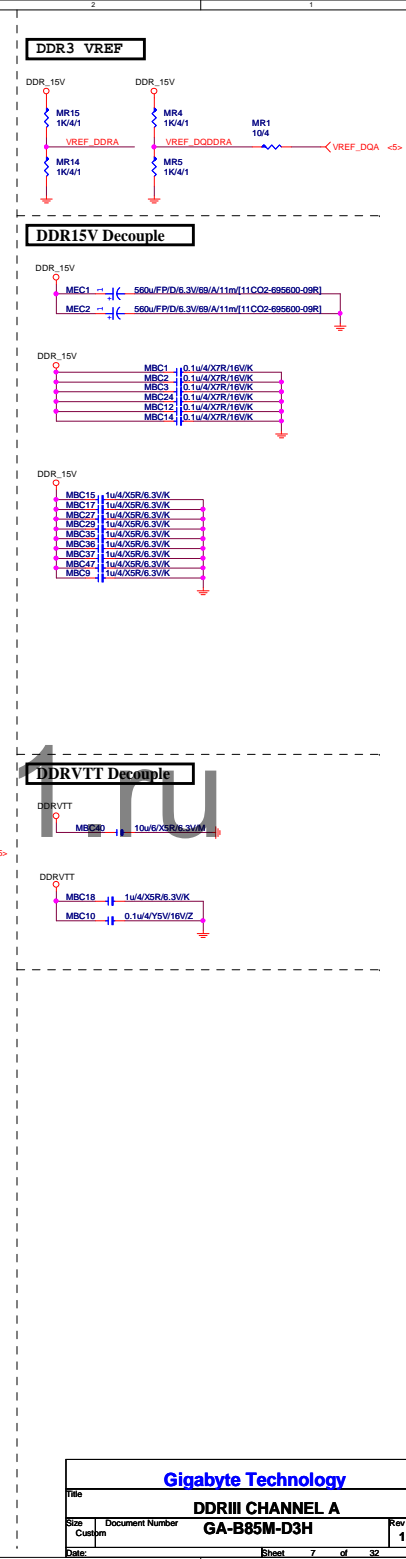
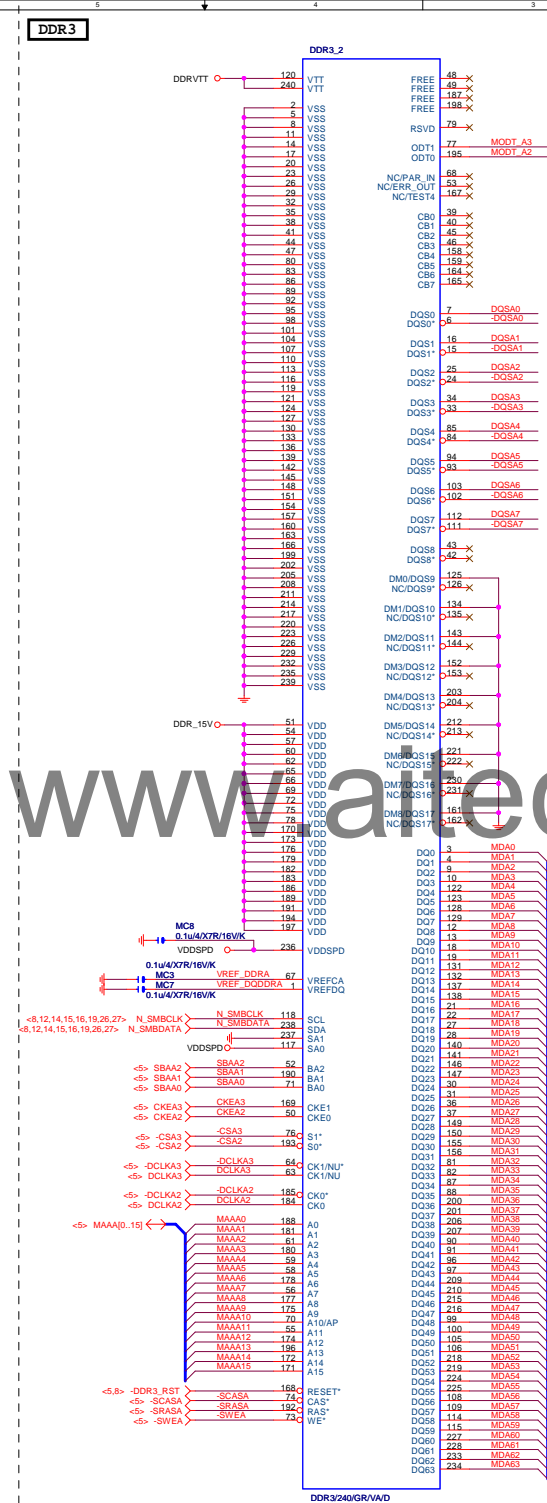
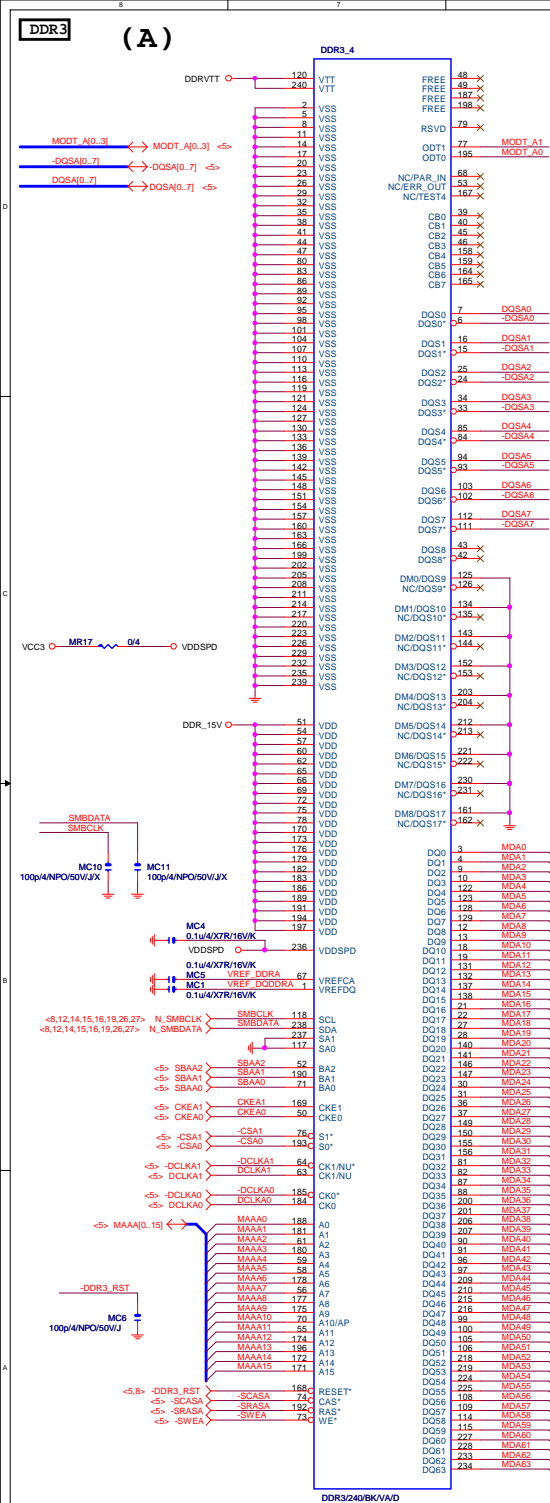
(1.0V)



CPU LGA1150-C

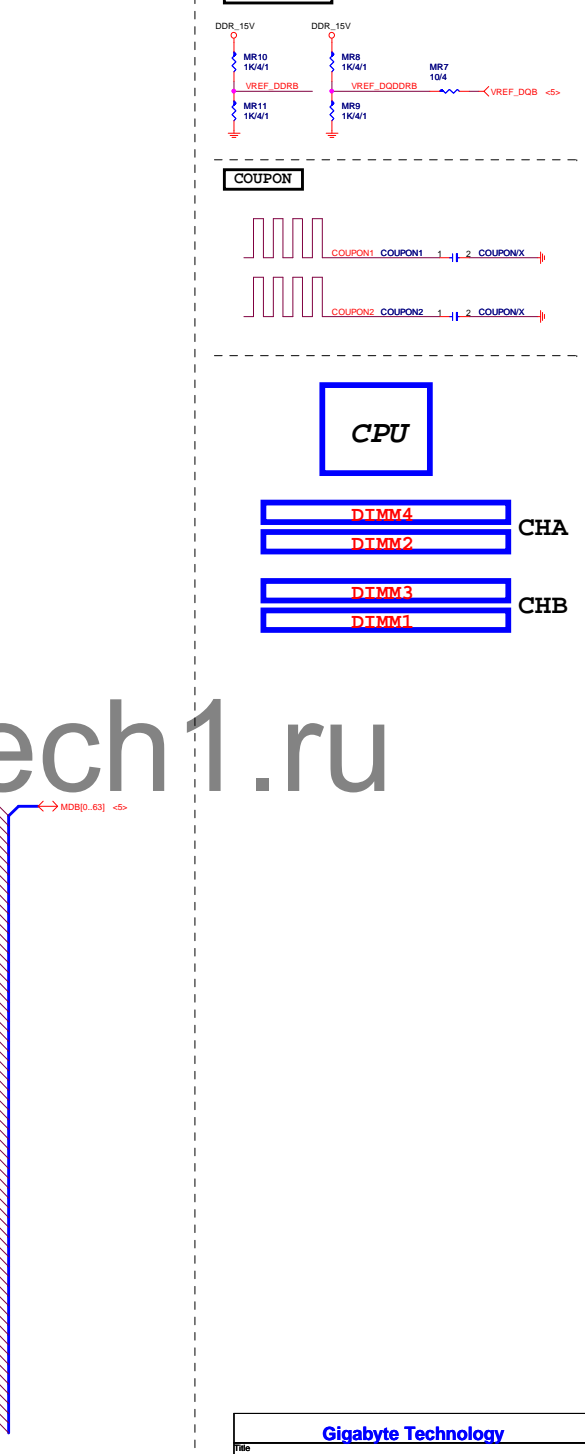
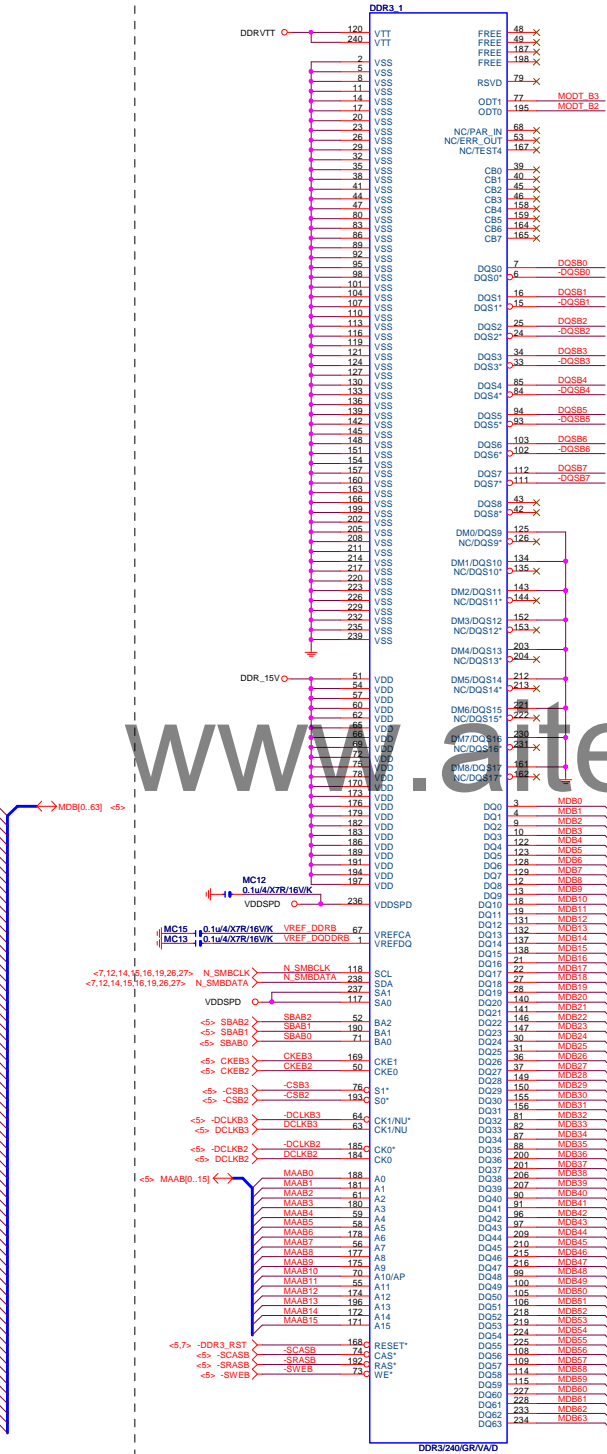
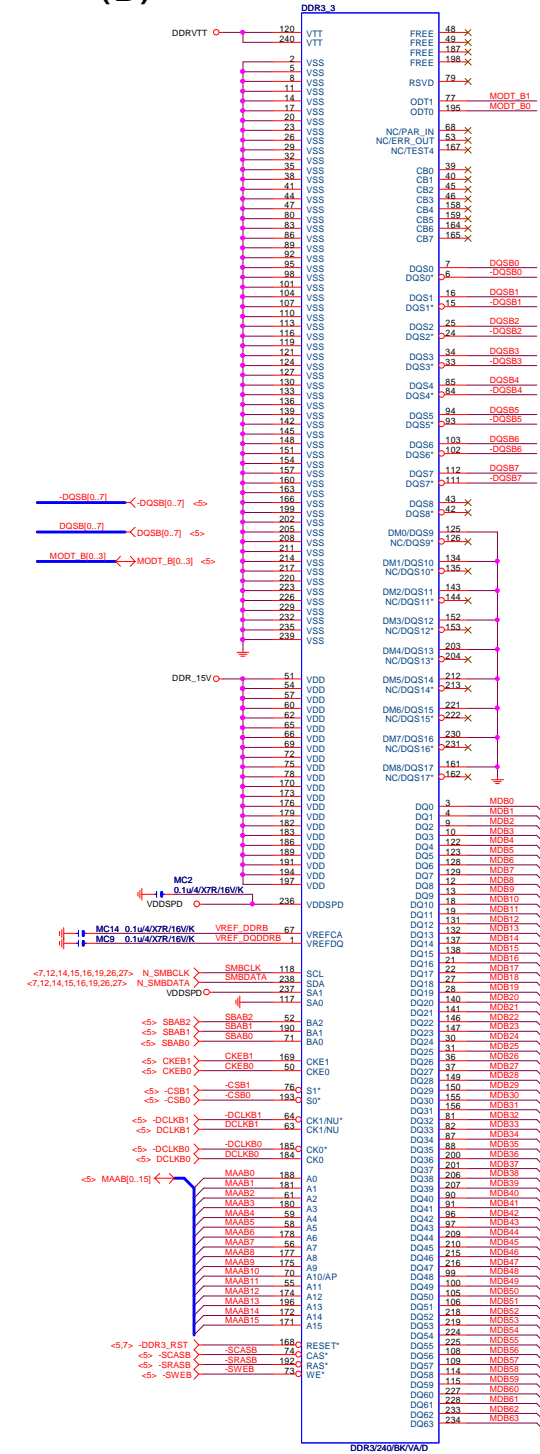
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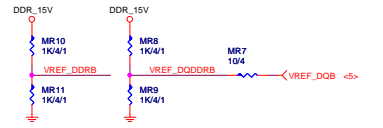


DDR3

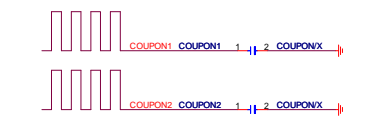
(B)



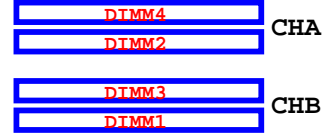
DDR3 VREF



COUPON



CPU



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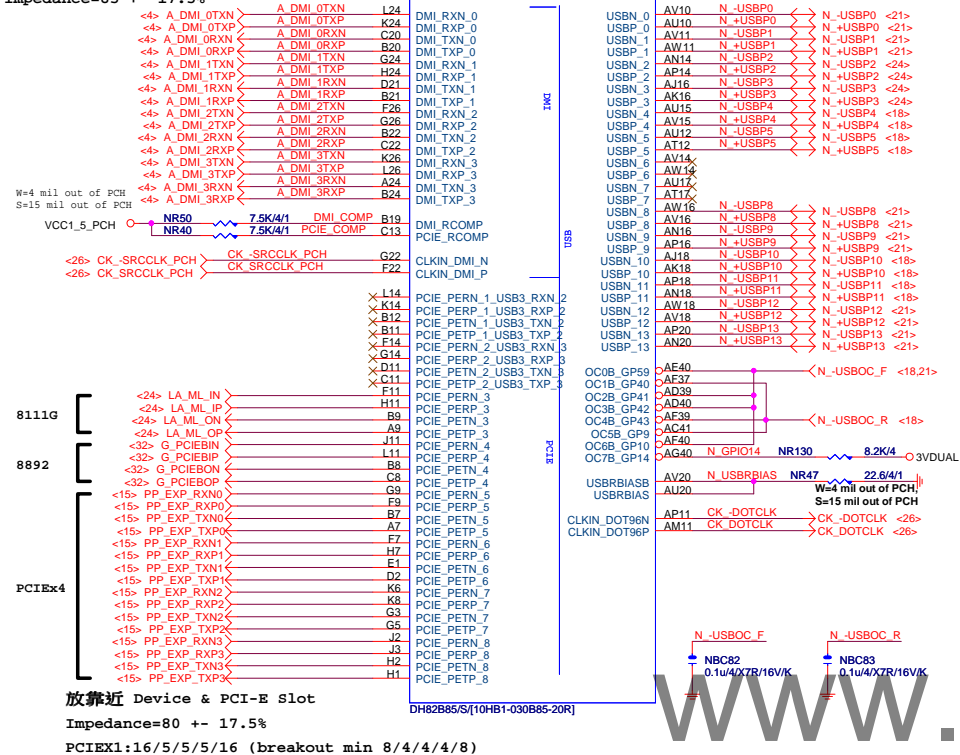
DMI:12/4/4/4/12(breakout min 8/4/4/4/8)
Impedance=85 +- 17.5%

USB2.0 : 12/4.5/7.5/4.5/12 (breakout min 8/4/4/4/8)
Impedance=90 +- 17.5%

PCHB

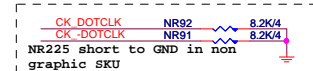
B85: Port 6/7 N/A

H81: Port 6/7/12/13 N/A



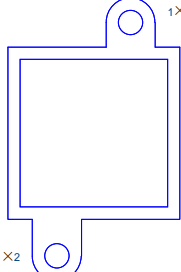
Timing diagram for USB3.0 signals. The diagram shows a VCC3.0 supply and several USB3.0 signals: RXN0, RXN1, RXN4, RXN5, RXN6, RXN7, TXN0, TXN1, TXN4, TXN5, TXN6, TXN7, TXP0, TXP1, TXP4, TXP5, TXP6, TXP7. The signals are shown as differential pairs (RXN, TXN) and (TXP, TXN). The timing is measured relative to a 100MHz clock. The signals are labeled with their respective pin numbers and signal names. The diagram shows the signals are sampled at 100MHz.

Mount for integrated clock Generation Mode



Pin connection diagram for the DH82B85/10HB1-030B85-20R1. The diagram shows a blue box labeled 'PCHU' with pins 1 through 28. Pins 1-10 are on the left, and pins 11-28 are on the right. Various pins are connected to external components: AT1, AT41, AU1, AV1, AV2, AV41, AW2, AW40, B40, B41, C41, D1, D41, TP22, TP23, TP21, TP20, TP14, TP15, TP12, TP10, TP11, TP9, TP3, TP2, TP5, TP6, TP7, TP8, VSS, VSS, VSS, and VSS. Some pins are crossed out with an 'X' and a label: U11, U10, AK15, AK14, K34, K33, AH29, L16, K16, AM39, R12, N12, L22, K22, R4, K5, P5, L5, AC31, AF3, and AV21. The bottom of the diagram is labeled 'DH82B85/10HB1-030B85-20R1'.

SB_HEATSIN



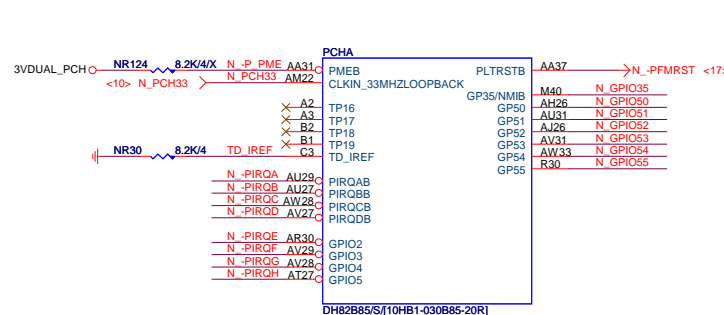
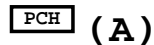
PCH_HS
PCH_HS[12SP2-S04209-01R_12SP2-S04209-02R_12SP2-S04209-03R]

```
OC[3:0]# for Device 29 (ports 0-7)
OC[7:4]# for Device 26 (ports 8-13)
```

USB OC# Configure	
OC0#	F_USB30
OC1#	F_USB1
OC2#	F_USB2
OC3#	F_USB3
OC4#	USB_LAN
OC5#	R_USB30
OC6#	KB_MS_USB
OC7#	Not Use

Title			
PCH FDI,DMI,USB ,PCIE,NVRAM			
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SATA3 : 20/7.5/4.5/7.5/20 (breakout min 8/4/4/4/8)
Impedance=90 +- 17.5%
SATA2 : 15/7.5/4.5/7.5/15 (breakout min 8/4/4/4/8)
Impedance=90 +- 17.5%



CK_SRCCLK SATA NR174 8.2K/4
CK -SRCCLK SATA NR173 8.2K/4

Mount for integrated Clock Generator Mode

Figure 1 shows the pin connections for the NR53 and NR55 comparators. The comparators are connected to a VCC3 supply. The output pins are connected to a 1K/4/1X resistor network. The input pins are connected to a 8.2K/8P/4R/4 resistor network.

Pin	Signal	Value
1	N-PIROQ	8.2K/8P/4R/4
2	N-PIROB	8.2K/8P/4R/4
3	N-PIROE	8.2K/8P/4R/4
4	N-PIROD	8.2K/8P/4R/4
5	N-PIROA	8.2K/8P/4R/4
6	N-PIROB	8.2K/8P/4R/4
7	N-PIROE	8.2K/8P/4R/4
8	N-PIROD	8.2K/8P/4R/4
9	N-GPIO6	1K/4/1X
10	N-GPIO5	1K/4/1X
11	N-GPIO5	1K/4/1X
12	N-GPIO6	1K/4/1X

SATA3 0_1

Diagram showing the SATA3 0_1 pinout. The central component is a blue square with four pins labeled TXP, TXN, RXN, and RXP. The connections are as follows:

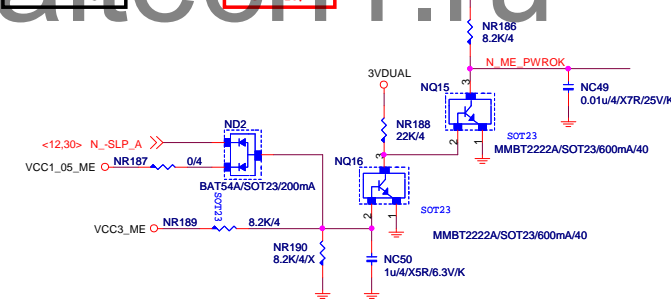
- TXP:** Pin 8 (GND) to NC42 (N SATA1TXP_0.01u4/X7R/25V/K), Pin 9 (TXP+) to NC44 (N SATA0TXPC), Pin 10 (TXN-) to NC43 (N SATA0TXNC).
- TXN:** Pin 9 (TXP+) to NC44 (N SATA0TXPC), Pin 10 (TXN-) to NC43 (N SATA0TXNC).
- RXP:** Pin 11 (RXN-) to NC38 (N SATA0RXNC), Pin 12 (RXN+) to NC37 (N SATA0RXP), Pin 13 (RXN-) to NC38 (N SATA0RXNC), Pin 14 (RXN+) to NC37 (N SATA0RXP).
- RXN:** Pin 11 (RXN-) to NC38 (N SATA0RXNC), Pin 12 (RXN+) to NC37 (N SATA0RXP), Pin 13 (RXN-) to NC38 (N SATA0RXNC), Pin 14 (RXN+) to NC37 (N SATA0RXP).

SATA14/WH/H/OP/RA/D/2

Pin	Signal	Internal Label
1	GND	NC36
2	+5V	NC35
3	T-	NC30
4	T+	NC29
5	R-	NC30
6	R+	NC29
7	GND	NC31

Pin	Signal	Internal Label
1	GND	NC34
2	+5V	NC33
3	T-	NC32
4	T+	NC31
5	R-	NC32
6	R+	NC31
7	GND	NC33

Z87 N/A



(D)



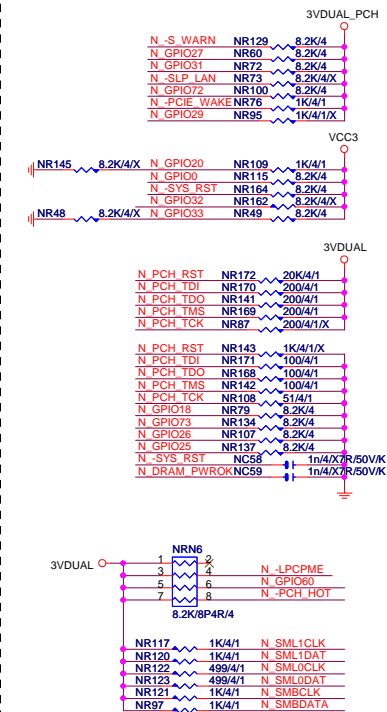
```
C_ACZ_SDOUT : HI --> ME Enable
              Lo --> ME Disable
HI:disable ME and override SOI Flash Access Permissions
```



Pinmux diagram for the 3VDDUAL pin. The diagram shows connections to various components and pins:

- NR155: 8.2K/4/X, N GPIO45
- NR139: 8.2K/4/X, N GPIO46
- NR103: 8.2K/4/X, N GPIO44, N GPIO57
- NR108: 1K/4/1, N _IGC EN
- NR153: 1K/4/1/X, N SUSCLK
- NR105: 8.2K/4/X
- NR154: 8.2K/4/X
- NR133: 8.2K/4/X
- NR51: 1K/4/1
- NR144: 1K/4/1
- NR96: 1K/4/1
- A_SKTOCC
- N_TEMP_ALARM

The 3VDDUAL pin is connected to pins 1, 2, 3, 4, 5, 6, 7, and 8 of these components. The diagram is labeled with GP8:Low to enable PCH clock chip, SUSCLK:Low to OD PLL VR, and GP28:Lo to disable VPM _Hi enable VPM.



NX2-SHT
SHW/D0.64*5.08*6.74

N Y1
N Y2

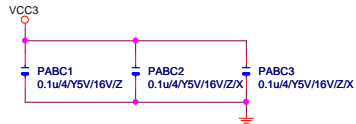
NR75 10M/4 NX2

32.768K/12.5p20ppm/TF38/35K/D

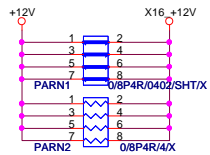
NC16 18P/4/NPO/50V/J NC18 18P/4/NPO/50V/J

Title			
PCH GPIO , CTRL , AUDIO			
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PCIEX16 CAP



PCIEX16 PROTECT SHT

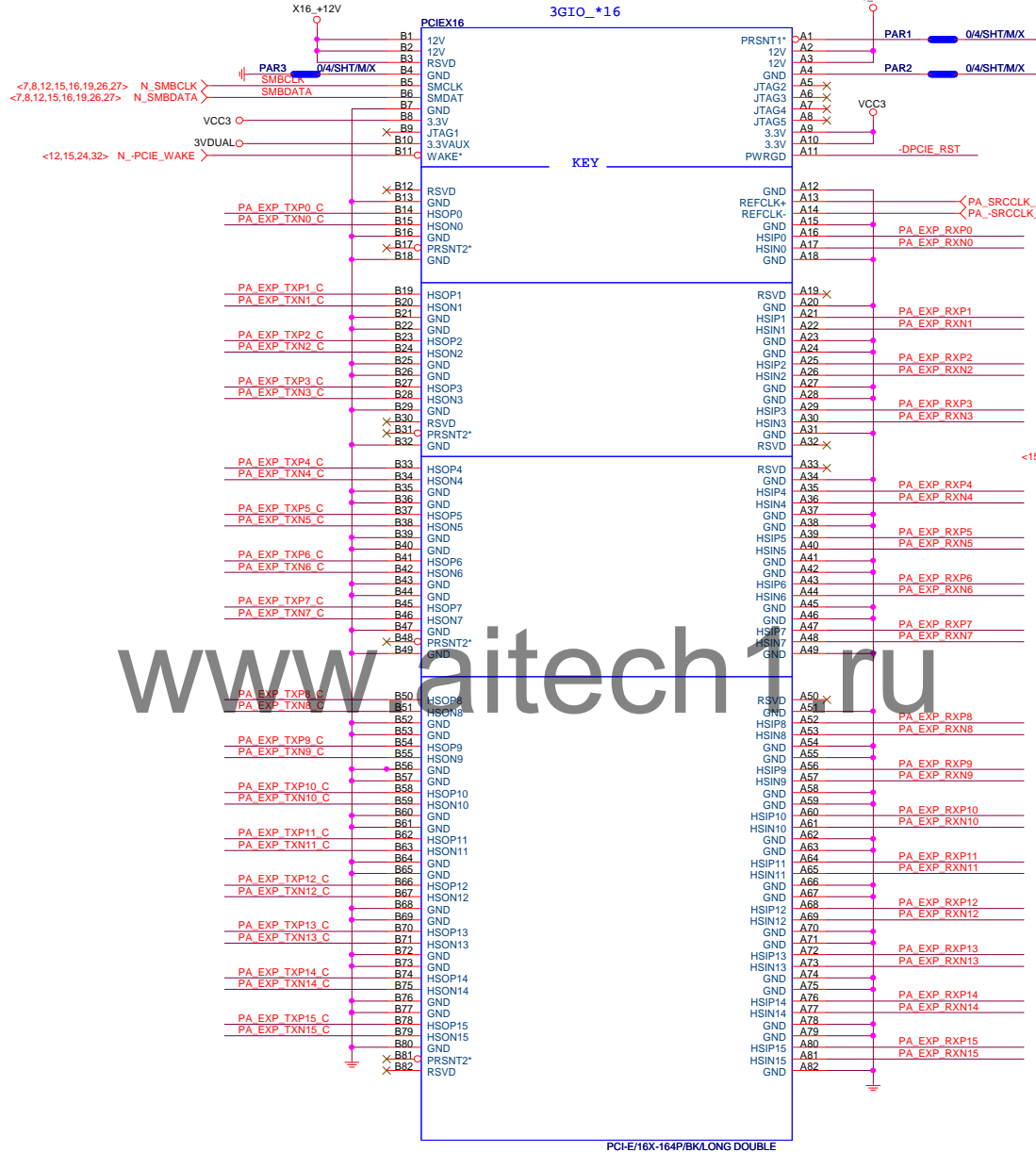


PCIEX16 AC CAP

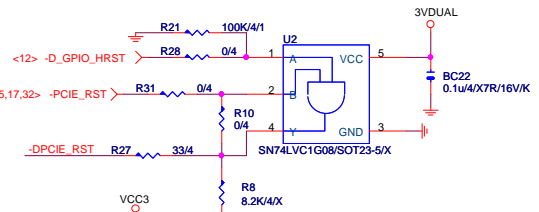
PA EXP TXP0	PAC5	0.22u4/X5R6.3V/K	PA EXP TXP0 C
PA EXP TXN0	PAC4	0.22u4/X5R6.3V/K	PA EXP TXN0 C
PA EXP TXP1	PAC6	0.22u4/X5R6.3V/K	PA EXP TXP1 C
PA EXP TXN1	PAC7	0.22u4/X5R6.3V/K	PA EXP TXN1 C
PA EXP TXP2	PAC8	0.22u4/X5R6.3V/K	PA EXP TXP2 C
PA EXP TXN2	PAC9	0.22u4/X5R6.3V/K	PA EXP TXN2 C
PA EXP TXP3	PAC10	0.22u4/X5R6.3V/K	PA EXP TXP3 C
PA EXP TXN3	PAC11	0.22u4/X5R6.3V/K	PA EXP TXN3 C
PA EXP TXP4	PAC12	0.22u4/X5R6.3V/K	PA EXP TXP4 C
PA EXP TXN4	PAC13	0.22u4/X5R6.3V/K	PA EXP TXN4 C
PA EXP TXP5	PAC14	0.22u4/X5R6.3V/K	PA EXP TXP5 C
PA EXP TXN5	PAC15	0.22u4/X5R6.3V/K	PA EXP TXN5 C
PA EXP TXP6	PAC16	0.22u4/X5R6.3V/K	PA EXP TXP6 C
PA EXP TXN6	PAC17	0.22u4/X5R6.3V/K	PA EXP TXN6 C
PA EXP TXP7	PAC18	0.22u4/X5R6.3V/K	PA EXP TXP7 C
PA EXP TXN7	PAC19	0.22u4/X5R6.3V/K	PA EXP TXN7 C
PA EXP TXP8	PAC20	0.22u4/X5R6.3V/K	PA EXP TXP8 C
PA EXP TXN8	PAC21	0.22u4/X5R6.3V/K	PA EXP TXN8 C
PA EXP TXP9	PAC22	0.22u4/X5R6.3V/K	PA EXP TXP9 C
PA EXP TXN9	PAC23	0.22u4/X5R6.3V/K	PA EXP TXN9 C
PA EXP TXP10	PAC24	0.22u4/X5R6.3V/K	PA EXP TXP10 C
PA EXP TXN10	PAC25	0.22u4/X5R6.3V/K	PA EXP TXN10 C
PA EXP TXP11	PAC26	0.22u4/X5R6.3V/K	PA EXP TXP11 C
PA EXP TXN11	PAC27	0.22u4/X5R6.3V/K	PA EXP TXN11 C
PA EXP TXP12	PAC28	0.22u4/X5R6.3V/K	PA EXP TXP12 C
PA EXP TXN12	PAC29	0.22u4/X5R6.3V/K	PA EXP TXN12 C
PA EXP TXP13	PAC30	0.22u4/X5R6.3V/K	PA EXP TXP13 C
PA EXP TXN13	PAC31	0.22u4/X5R6.3V/K	PA EXP TXN13 C
PA EXP TXP14	PAC32	0.22u4/X5R6.3V/K	PA EXP TXP14 C
PA EXP TXN14	PAC33	0.22u4/X5R6.3V/K	PA EXP TXN14 C
PA EXP TXP15	PAC34	0.22u4/X5R6.3V/K	PA EXP TXP15 C
PA EXP TXN15	PAC35	0.22u4/X5R6.3V/K	PA EXP TXN15 C

PA EXP RXP[0..15] >>> PA_EXP_RXP[0..15] <4>
 PA EXP RXN[0..15] >>> PA_EXP_RXN[0..15] <4>
 PA EXP TXP[0..15] >>> PA_EXP_TXP[0..15] <4>
 PA EXP TXN[0..15] >>> PA_EXP_TXN[0..15] <4>

PCIEX16 SLOT



The auxiliary reset circuit is only required for PCIe Gen3 margining and functional link training



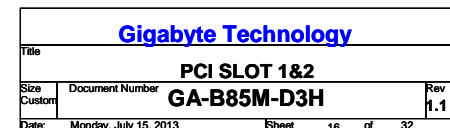
Gigabyte Technology			
Title PCI EXPRESS * 16			
Size Custom	Document Number GA-B85M-D3H	Rev 1.1	
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[illegible]

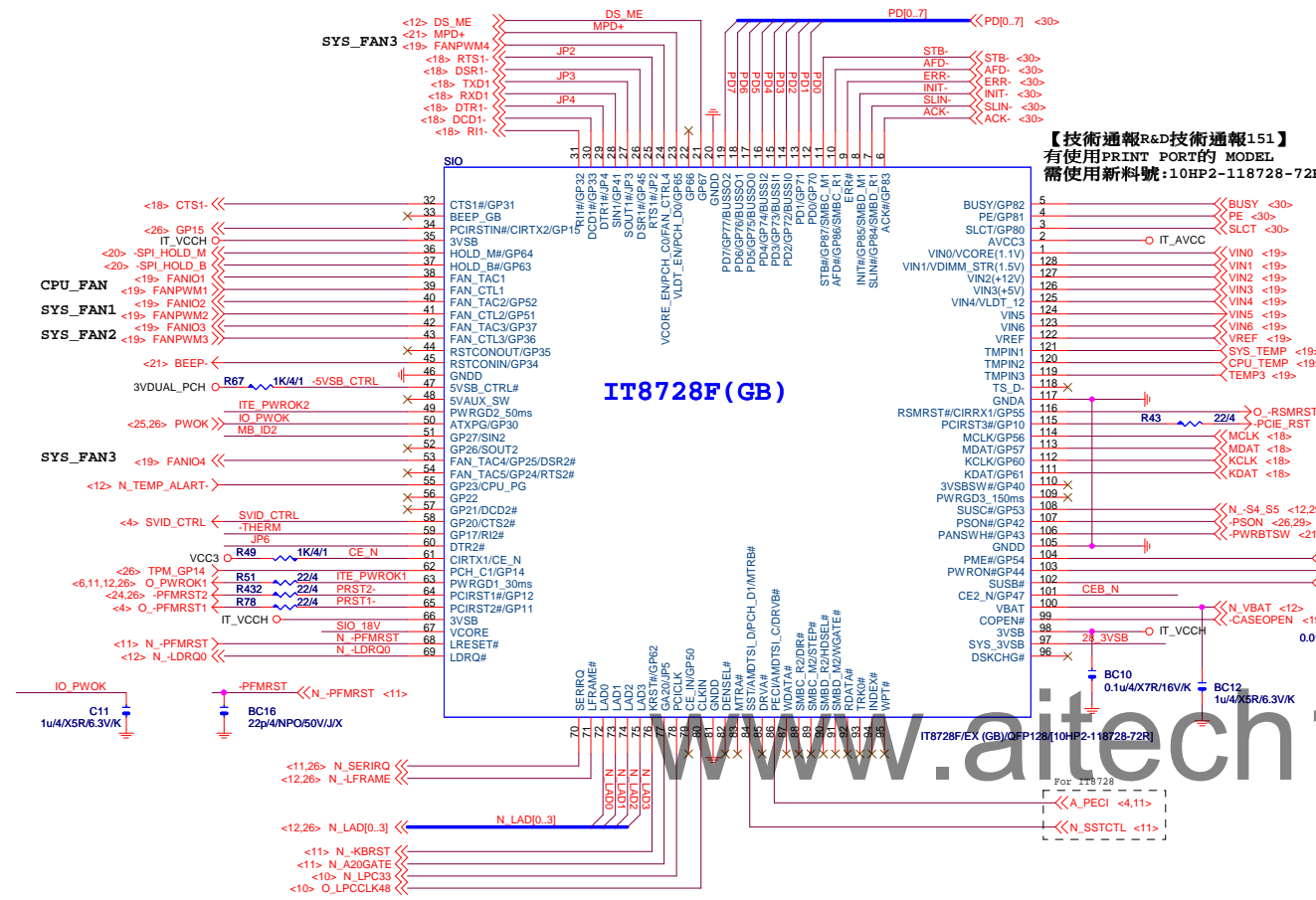
PCI SLOT 2	
------------	--



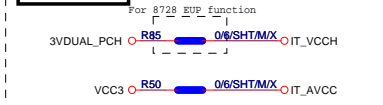
PCI CAP



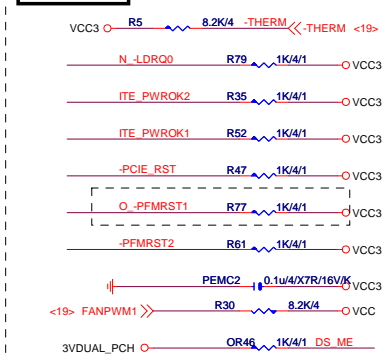
SIO IT8728F



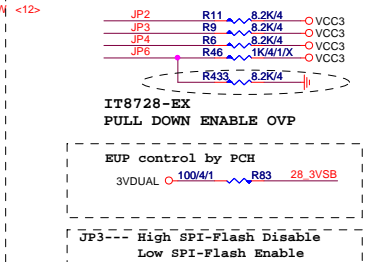
PWR SHT



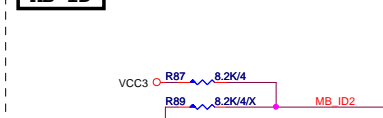
SIO PU



SIO STRAP



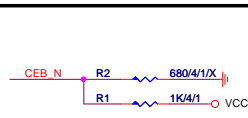
MB ID



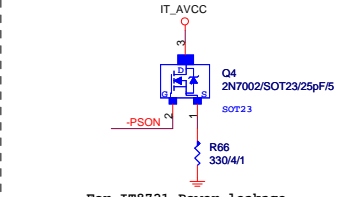
IT8728F NOTE

	IT8728
PIN121	VCORE_EN/PCH_C0
PIN120	VLDI_EN/PCH_D0
PIN19	ATXPG
PIN31	PCH_C1
PIN53	SST/AMDTSLI_D/MTRB# /PCH_D1
PIN55	PECI/AMDTSLI_C/DRV#
PIN66	SYS_3VSB
PIN70	GP47
PIN95	VIN2(VCC5)
PIN96	VIN1(VCC12)
PIN97	VIN1/VDIMM_STR(1.5V)
PIN98	VIN0/VCORE(1.1V)/NC

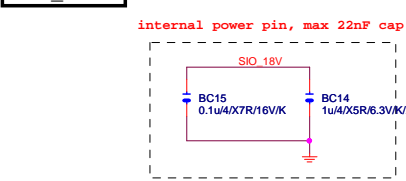
DUAL BIOS OPT STRAP



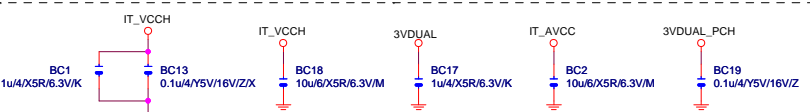
Power leakage



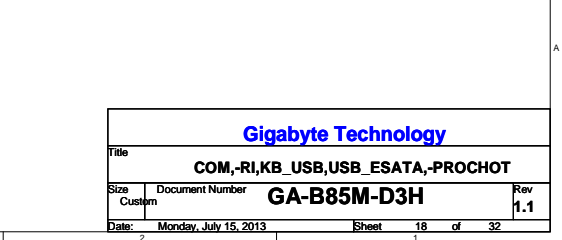
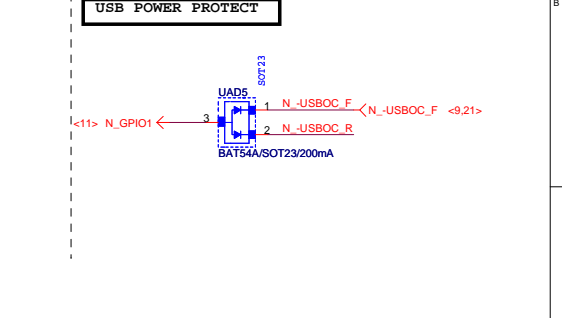
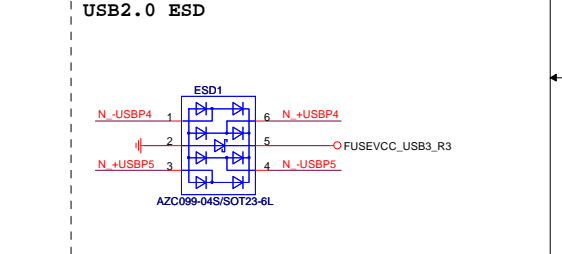
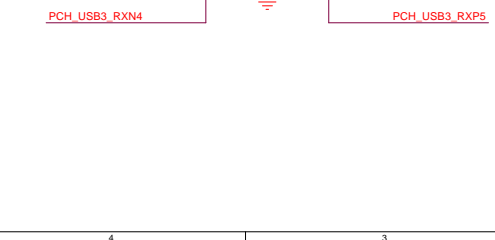
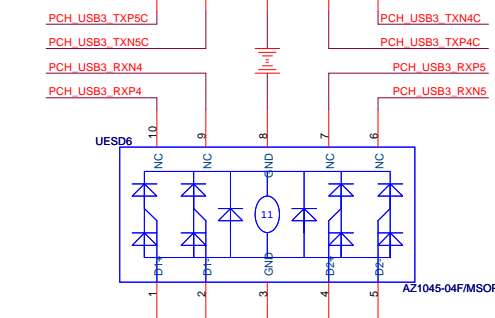
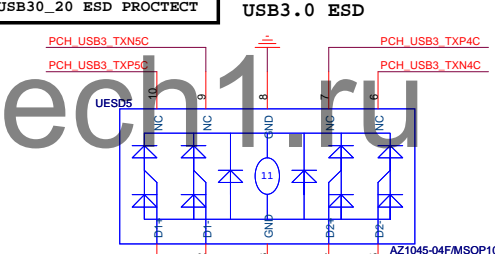
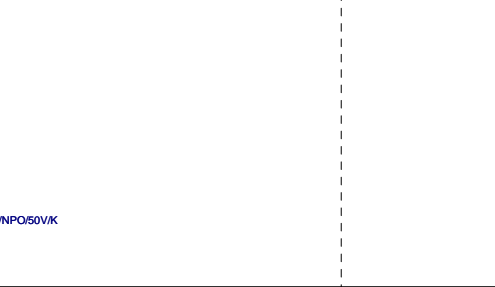
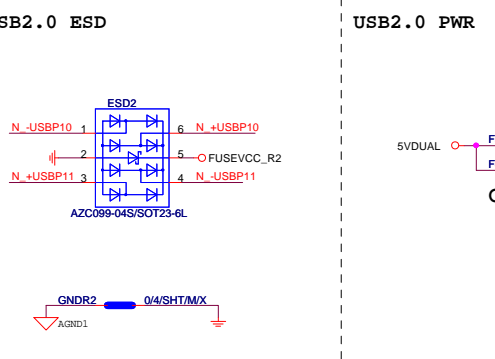
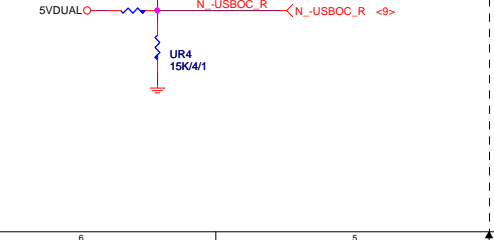
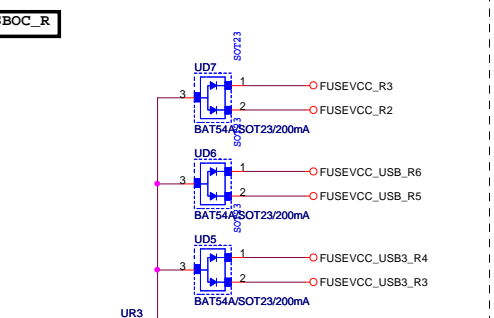
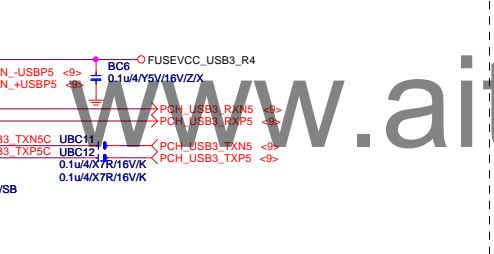
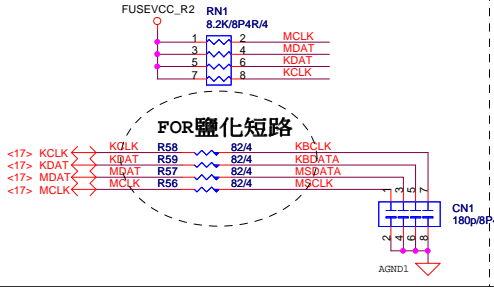
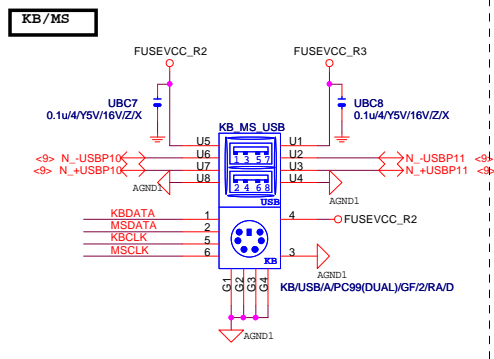
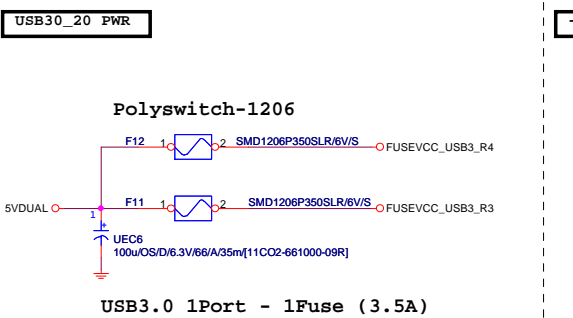
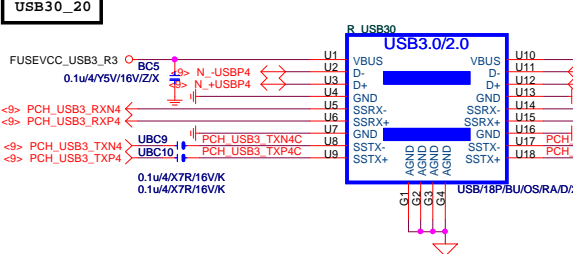
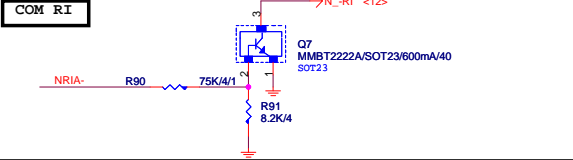
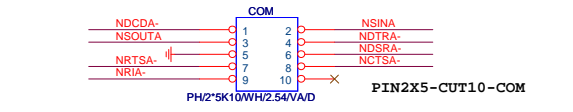
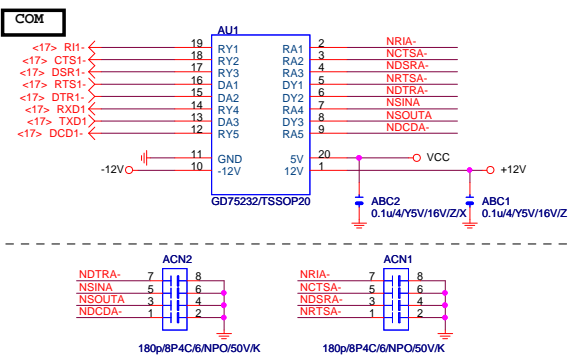
SIO_18V



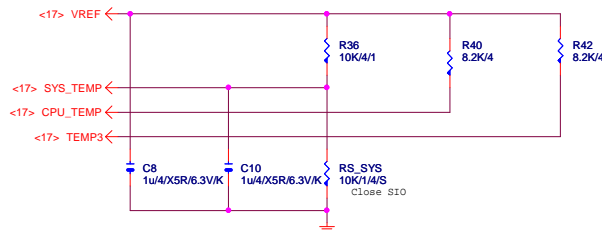
SIO CAP



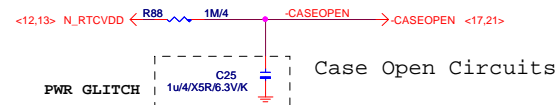
Gigabyte Technology			
Title	ITE 8728 LPC IO		
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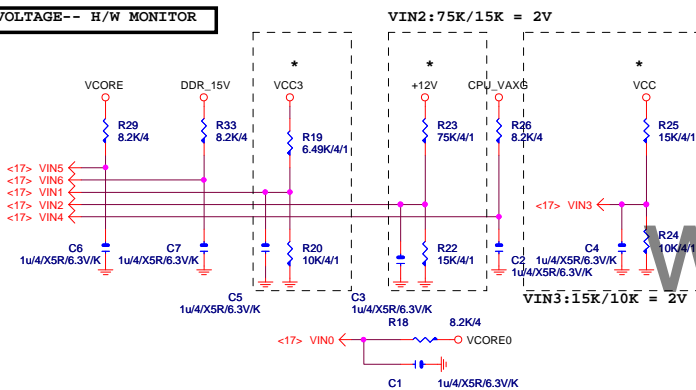
TEMP H/W MONITOR



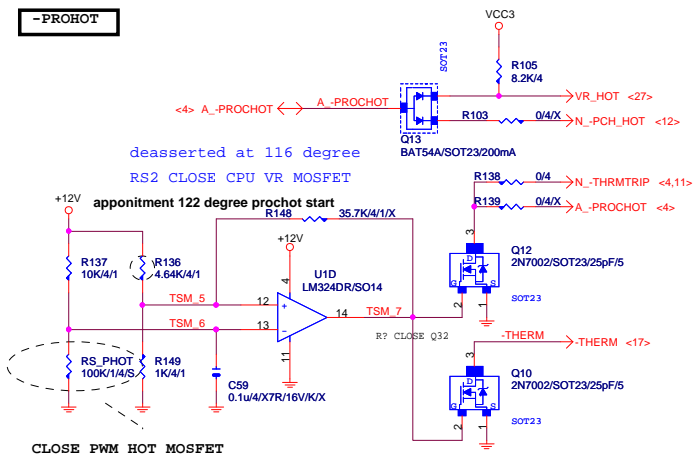
CASE OPEN



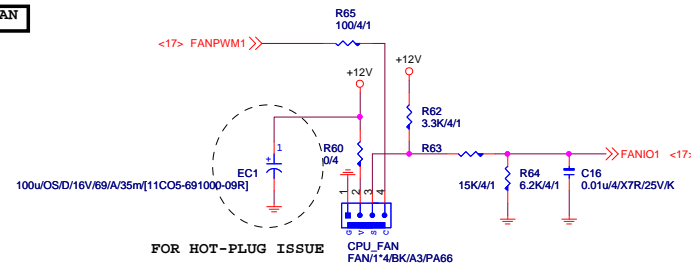
VOLTAGE-- H/W MONITOR



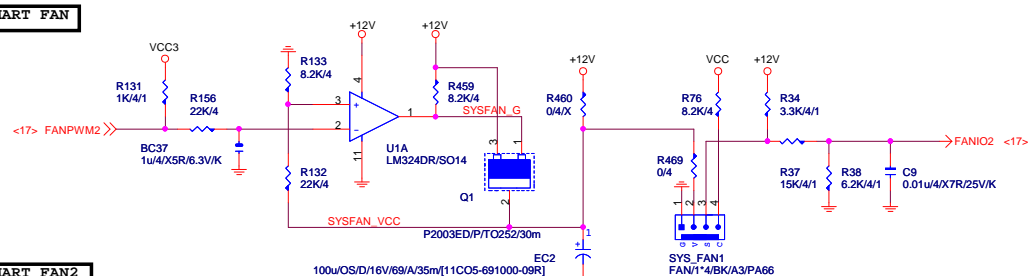
-PROHOT



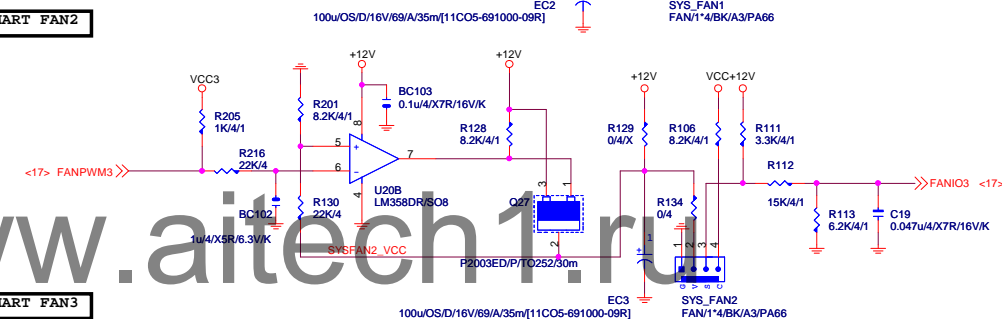
CPU SMART FAN



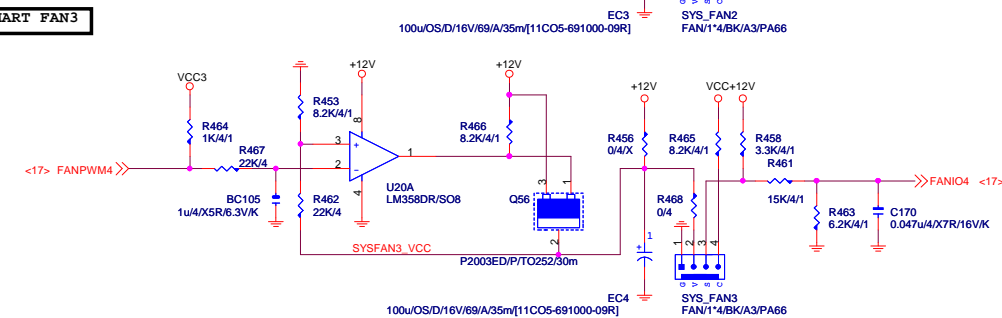
SYS SMART FAN



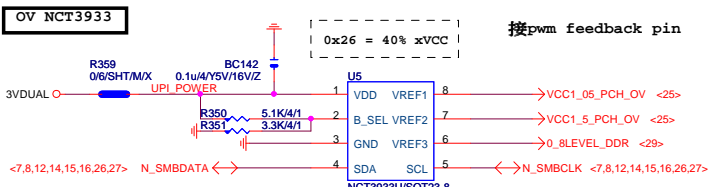
SYS SMART FAN2

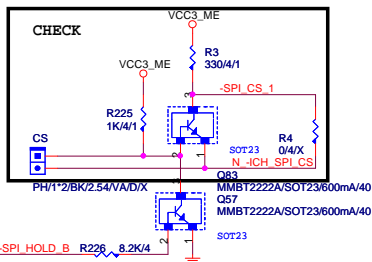
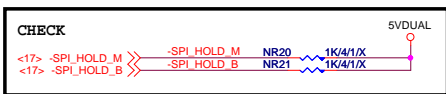
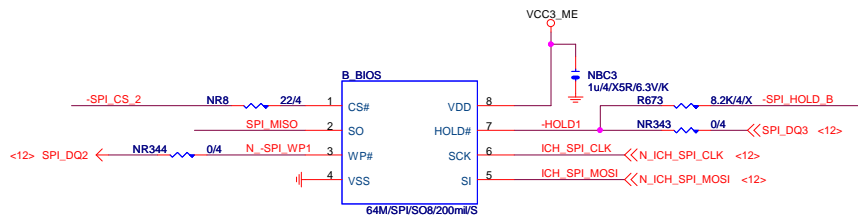
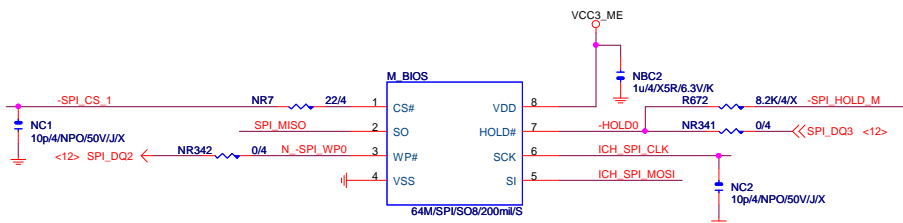


SYS SMART FAN3

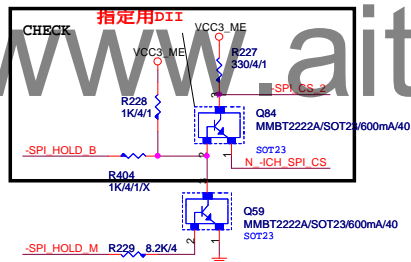


OV NCT3933



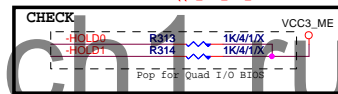
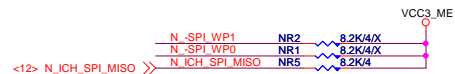
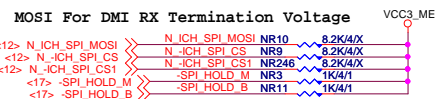


Dual BIOS CS connect
circuit update



BOOT DEVICE	GNT0	GNT1
LPC	0	0
PCI	0	1
NAND	1	0
SPI	1	1

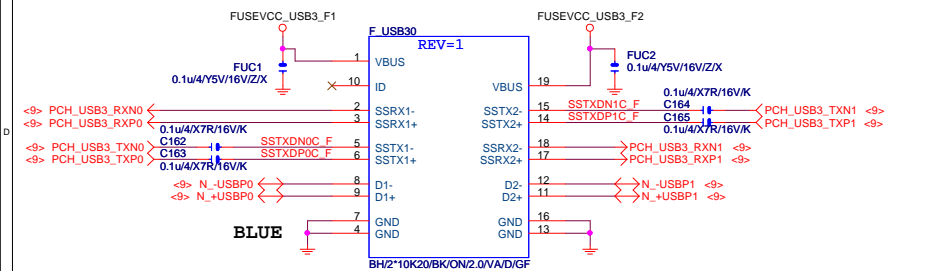
1 means floating
0 means PD 1k



Gigabyte Technology

Title			
DUAL BIOS			
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F_USB30



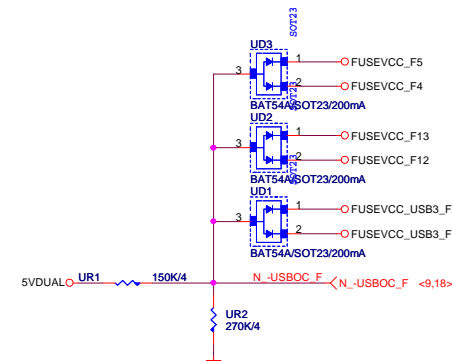
F_USB30	PWR
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Polyswitch-1206

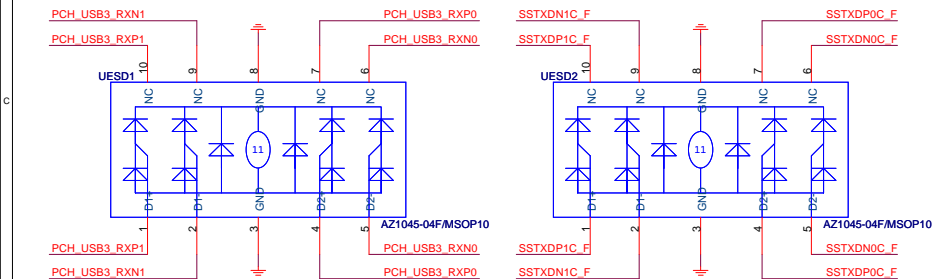


USB3.0 1Port - 1Fuse (3.5A)

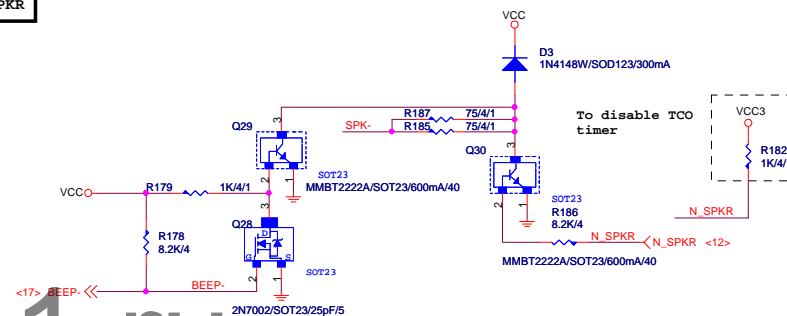
-USB0C_F



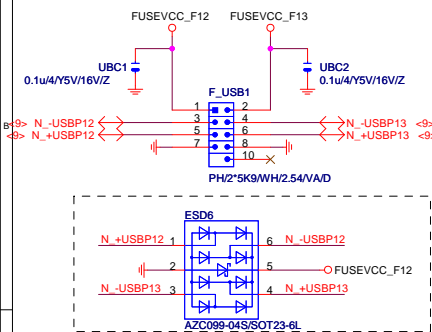
F_USB30 ESD PROTECT



SPKR

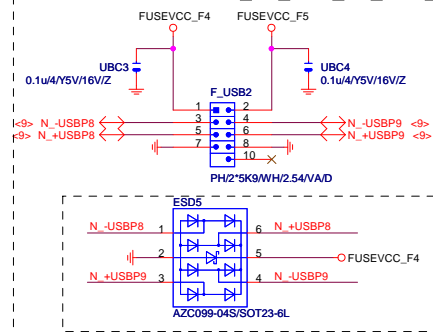


FRONT USB1



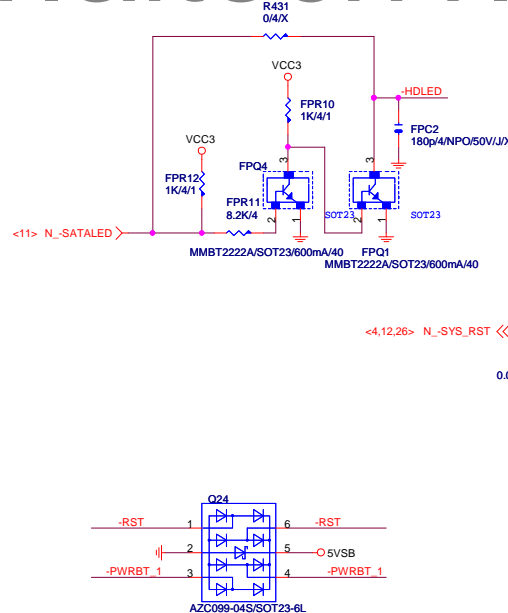
Close to connector

FRONT USB2

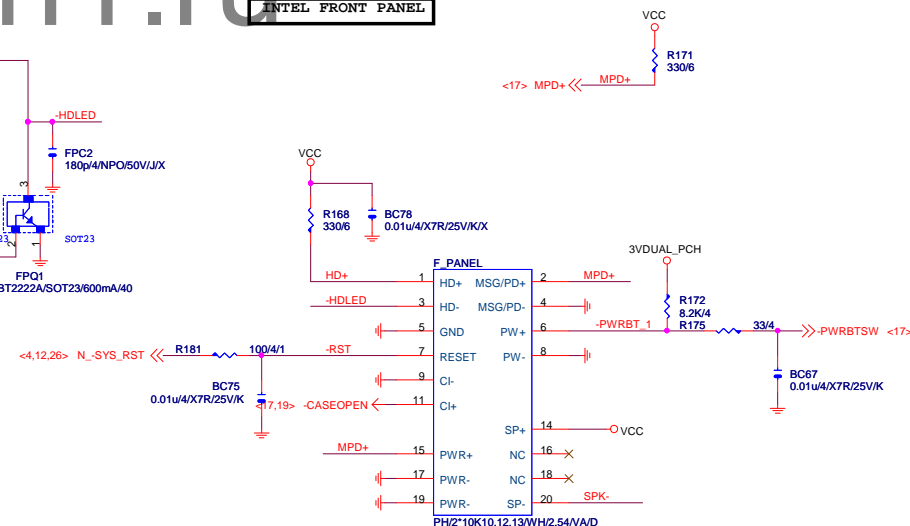


Close to connector

SATA LED



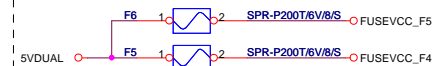
INTEL FRONT PANEL



FUSE-0805

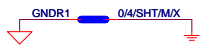
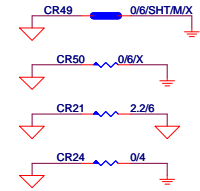


FUSE-0805

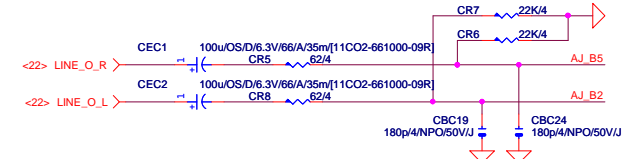


ALC892/ALC887-VD2/VT1708-CE Colay





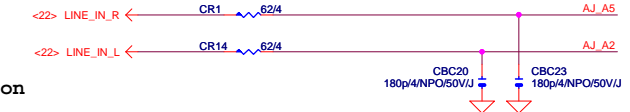
LINE-OUT



Only reserved for ALC888

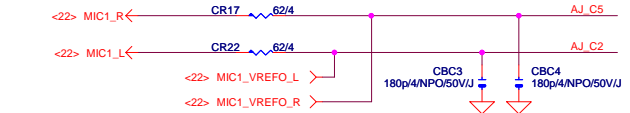
LINE-IN

Verify MIC function
in LINE-in

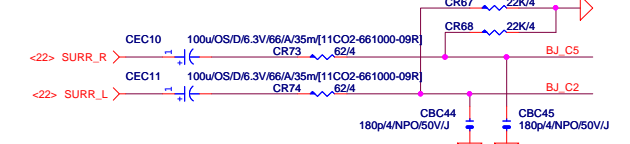


For 889A/888

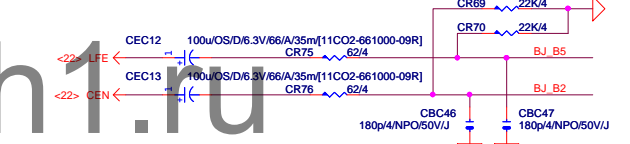
MIC-IN



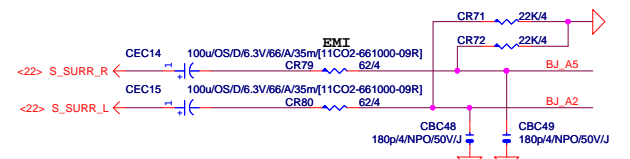
SURROUND



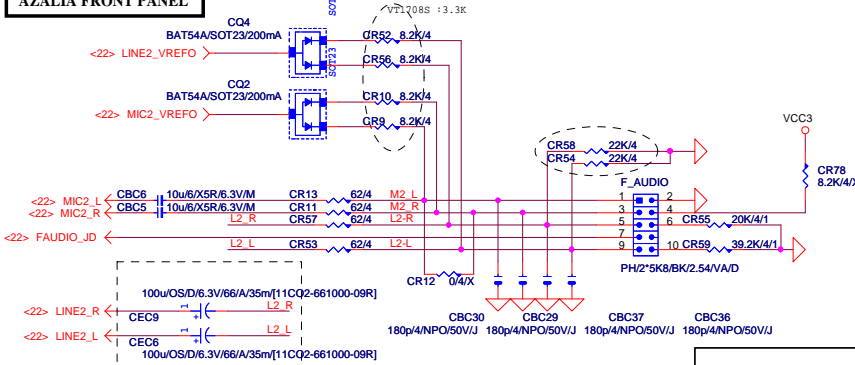
CEN/LFE



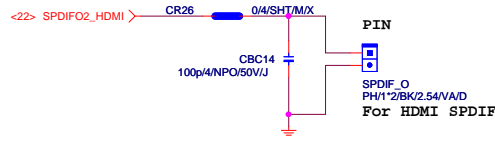
SURR BACK



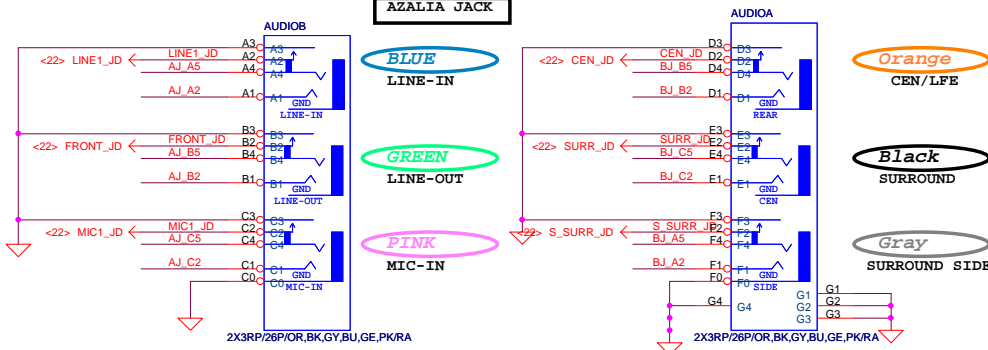
AZALIA FRONT PANEL



SPDIF_OUT



AZALIA JACK



Gigabyte Technology

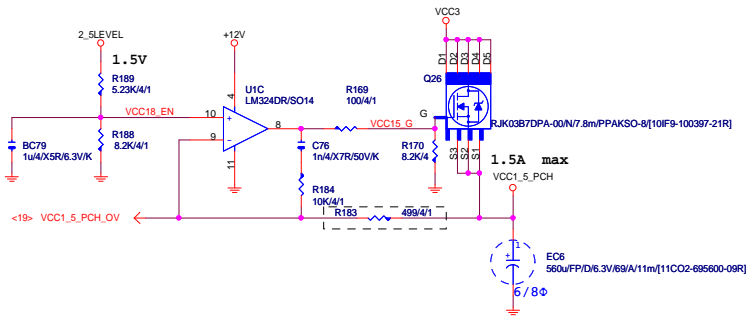
AUDIO JACK

GA-B85M-D3H

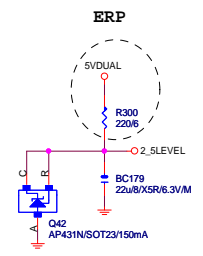
Rev 1.1

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Date	Sheet 23	of 32

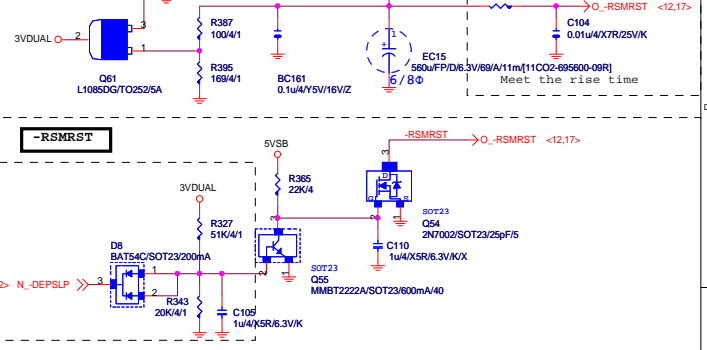
VCC1_8_PCH



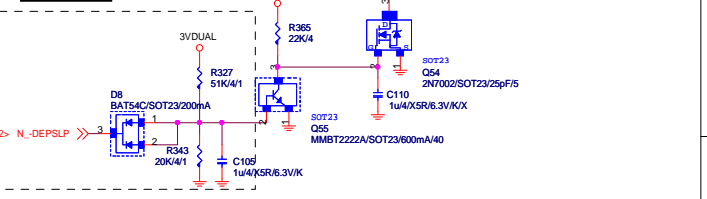
2_5LEVEL



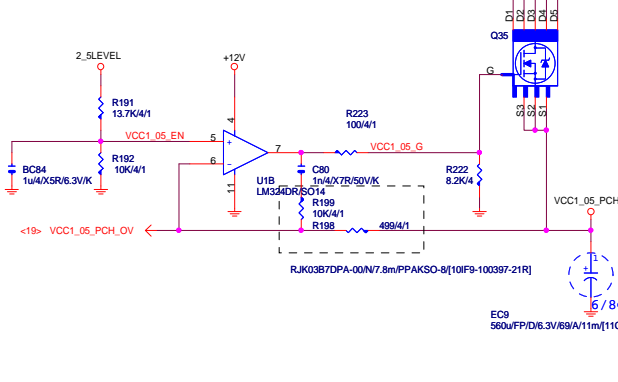
3VDUAL



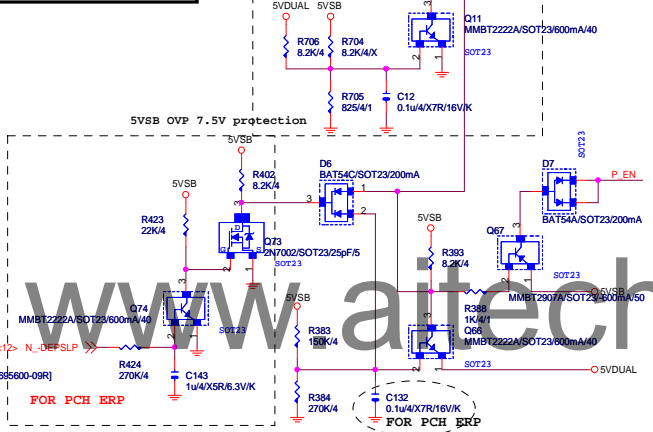
-RSMRST



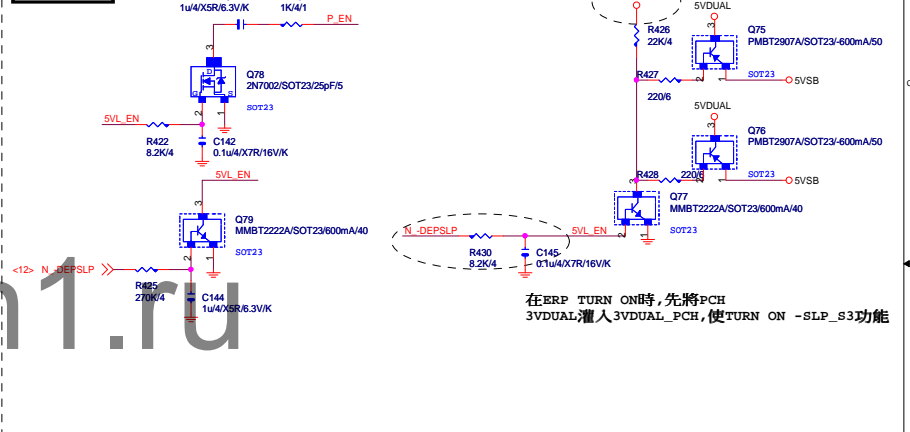
VCC1_05_PCH



5VDUAL SHORT PROTECT

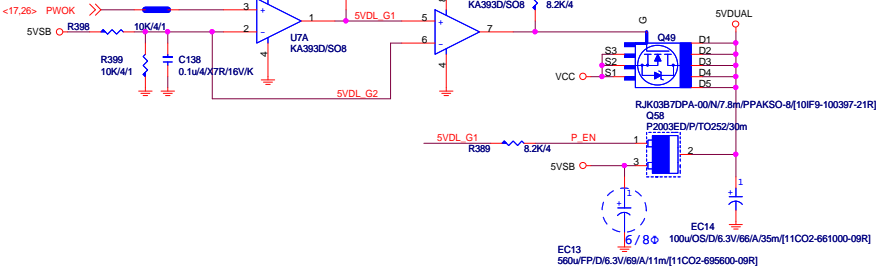


PCH ERP

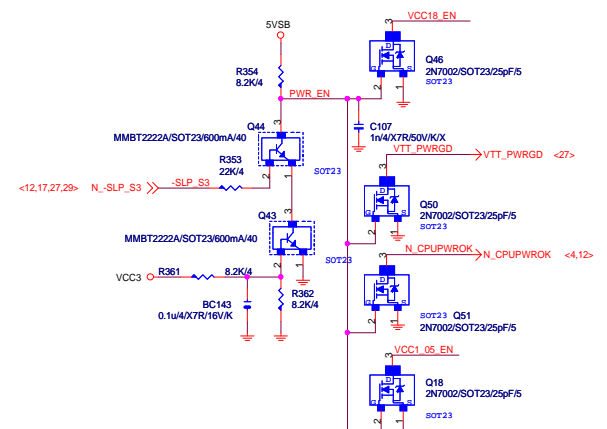


在ERP TURN ON時, 先將PCH 3VDUAL灌入3VDUAL_PCH, 使TURN ON -SLP_S3功能

5VDUAL



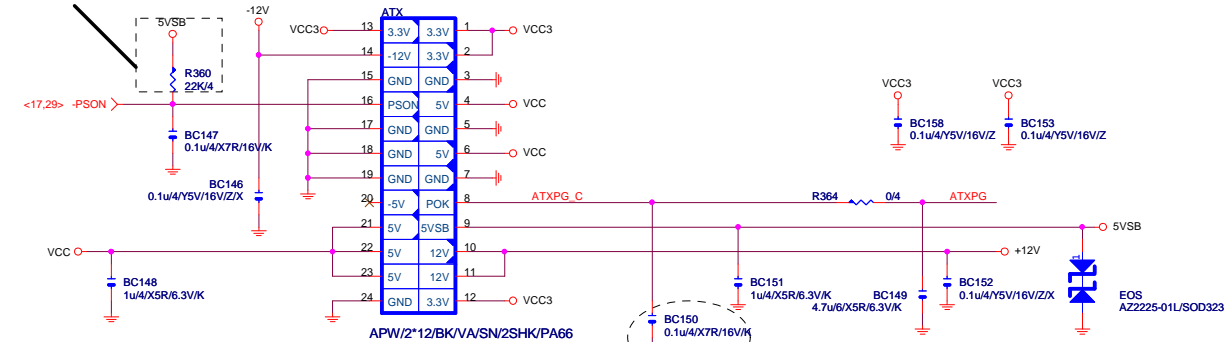
PWR SEQ



Gigabyte Technology			
Title			
DISCRETE POWER			
GA-B85M-D3H			
Size	Document Number	Rev	
Custom		1.1	
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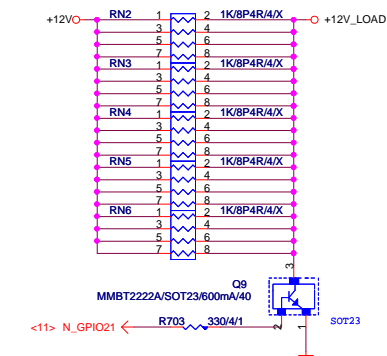
ATXX24 POWER CONNECTOR

【技術通報R&D技術通報155】



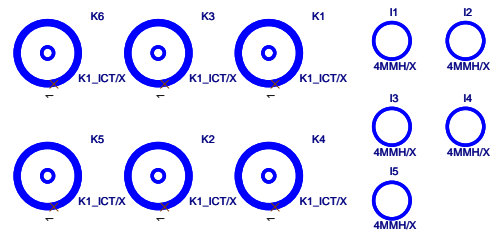
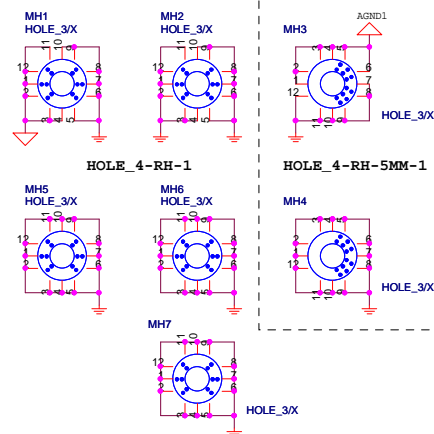
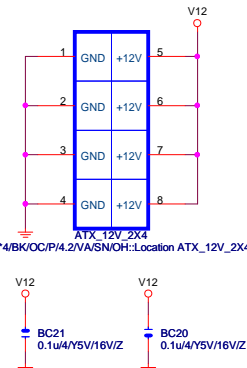
【技術通報R&D技術通報153】

To fix 12V light load abnormal issue



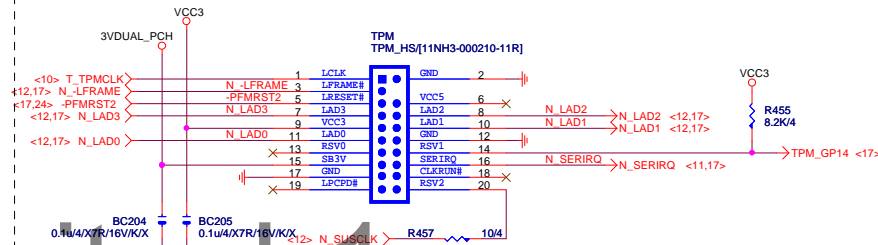
ATXX4 POWER CONNECTOR

APW/2*4BK/OC/PI4.2V/AS/NOH:1 Location ATX_12V_2X4



To prevent the 5VSB under loading when boot

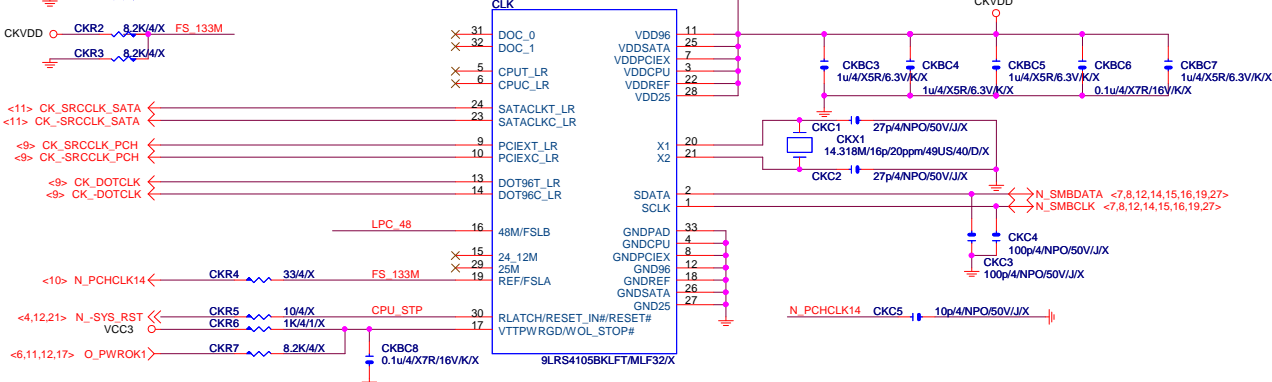
TPM



CLK GEN

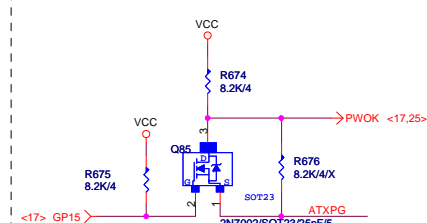
CPU Frequency Selection

FSLB	FSLA	CPU
0	0	100M <Default>
0	1	133M
1	0	200M
1	1	166M



PWOK PATCH

【技術通報R&D技術通報154】



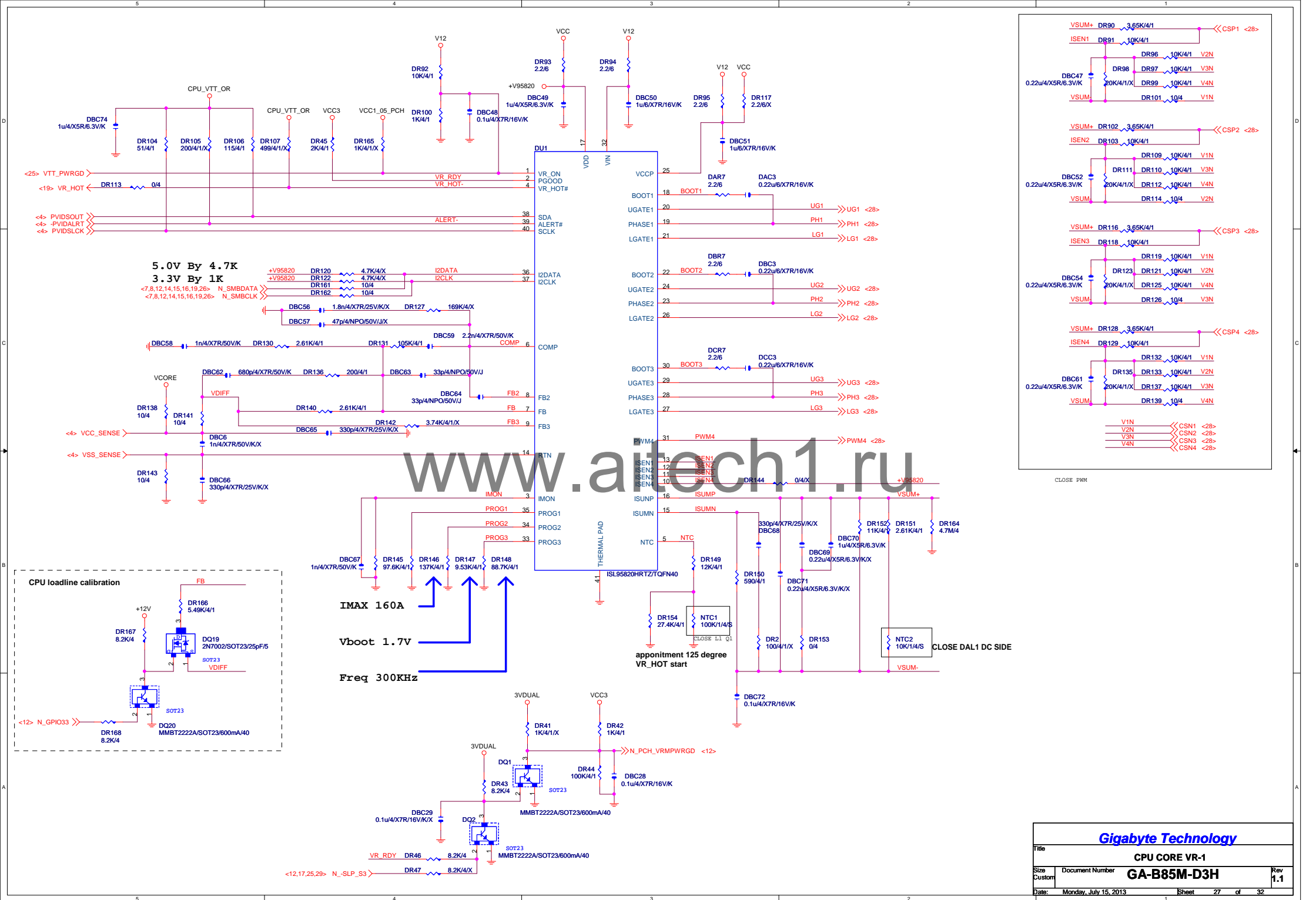
Gigabyte Technology

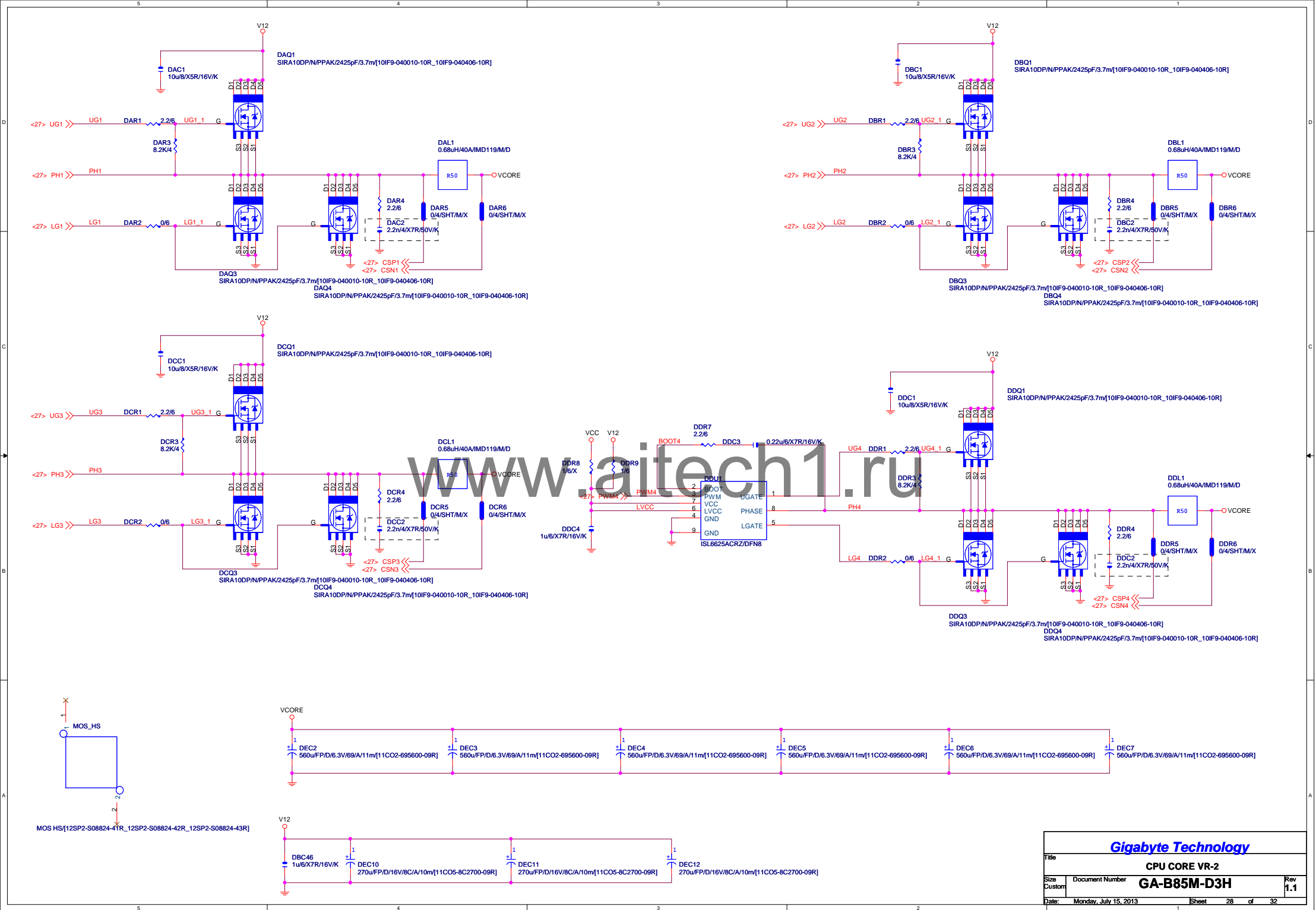
ATX CONNECTOR

GA-B85M-D3H

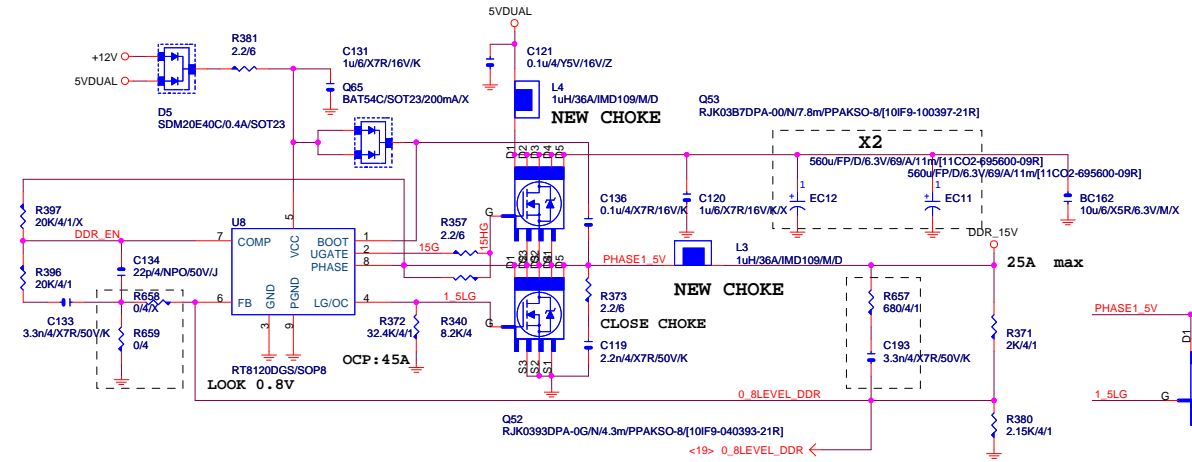
Rev 1.1

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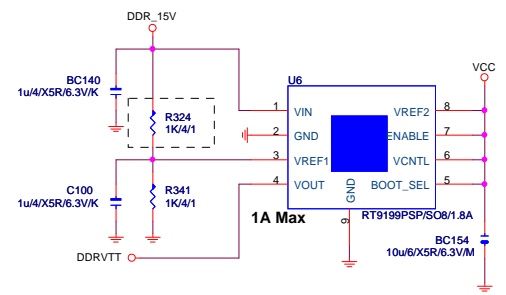




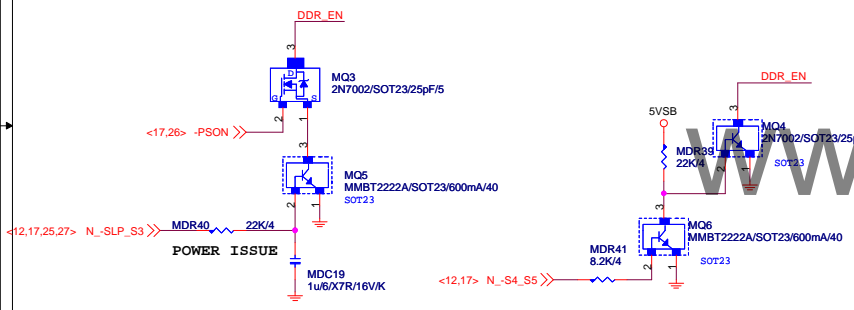
DDR15V



DDRVRTT

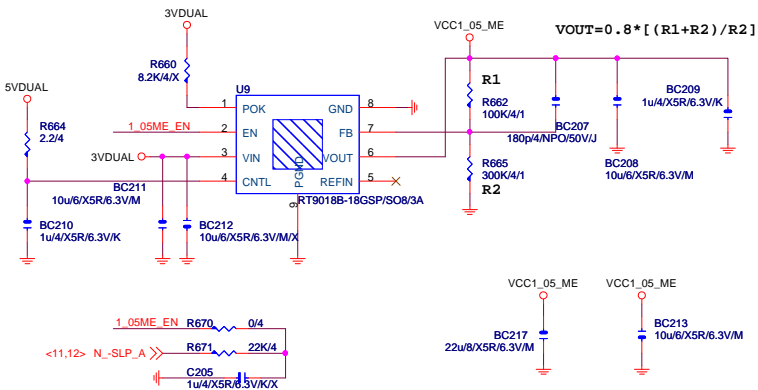


PWR SEQ

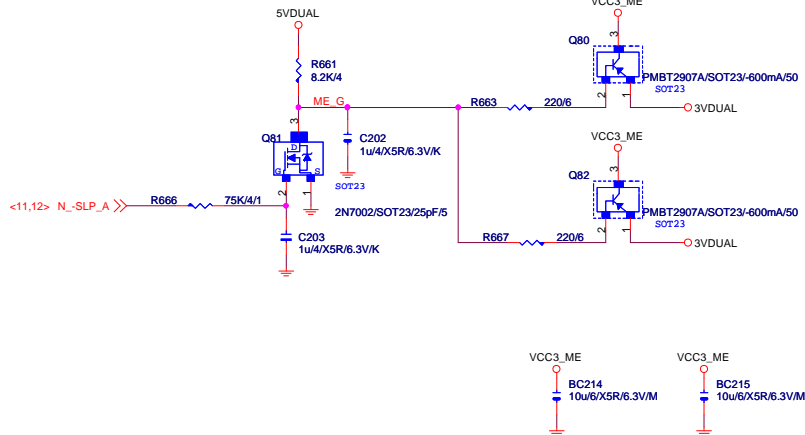


VIN=5V, VOUT=1.5V, IOUT=25A, PHASE=1
 IRMS=11.45A
 560u/FP/D/6.3V/68/8m RIPPLE CURRENT=4.7A
 Coefficient=1.7(85°C), 1(105°C)
 VIN Ripple current=4.7X1.7=7.99A(85°C)
 -->故固态电容须2X7.99=15.98>11.45A
 $R_{ocset} = (I_{ocp} * L_{gate} + r_{dson}) / I_{ocset}$
 $R_{ocset} = (45A * 6.7m\Omega + 10\mu A) / 30K$
 $I_{ocset} = 10\mu A$

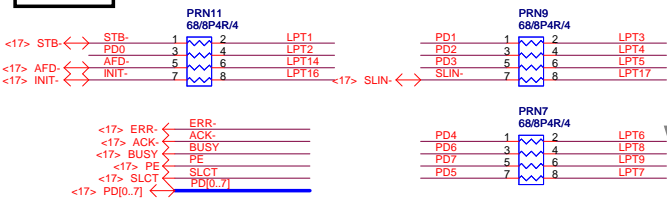
VCC1_05_ME



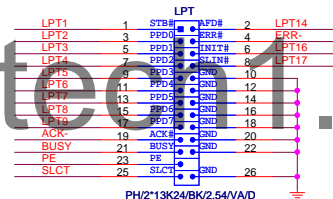
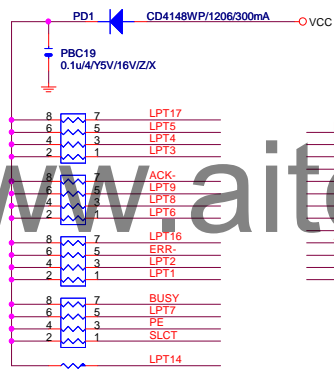
VCC3_ME



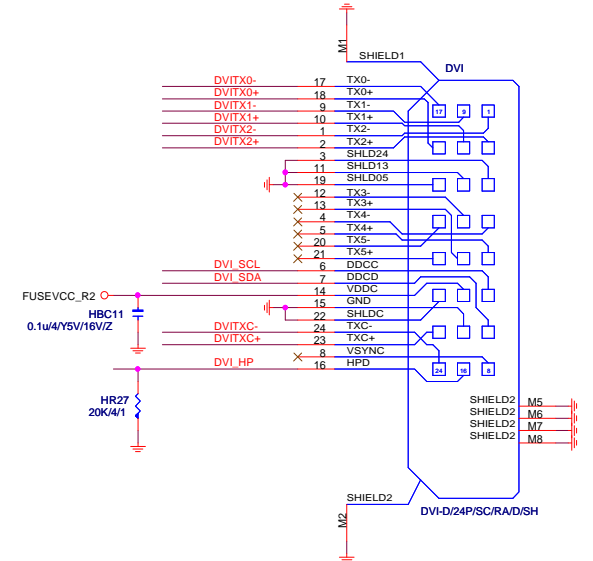
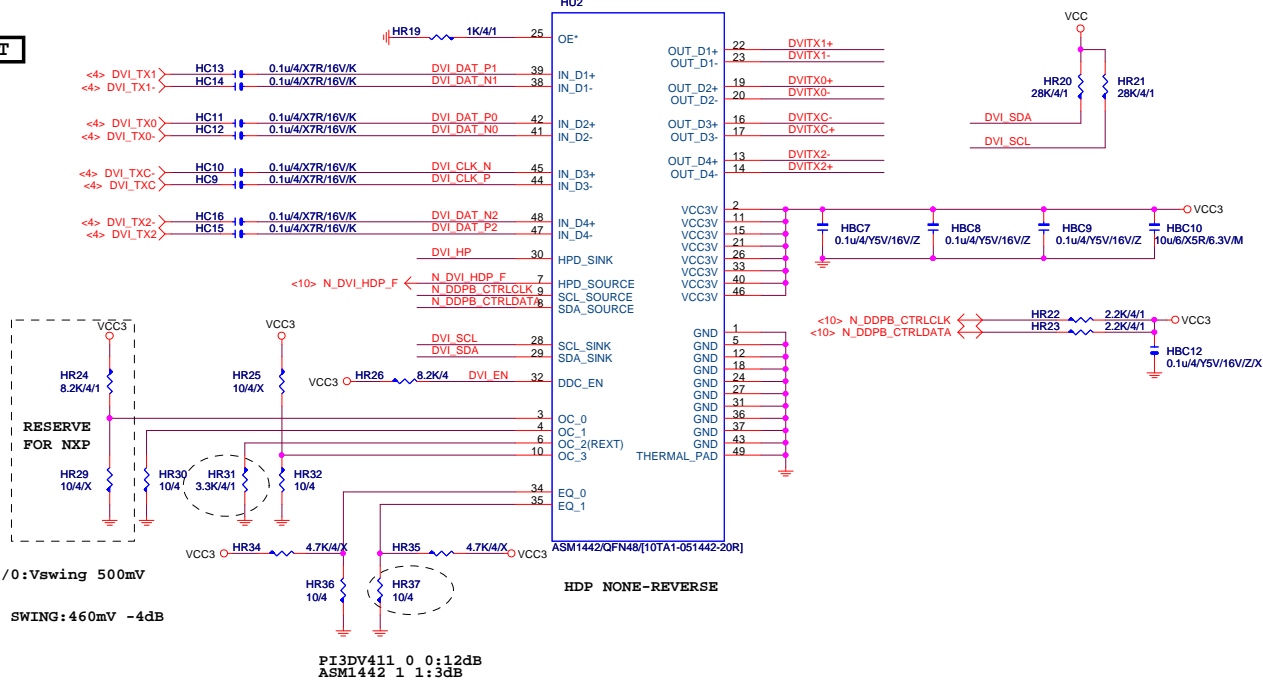
LPT PORT



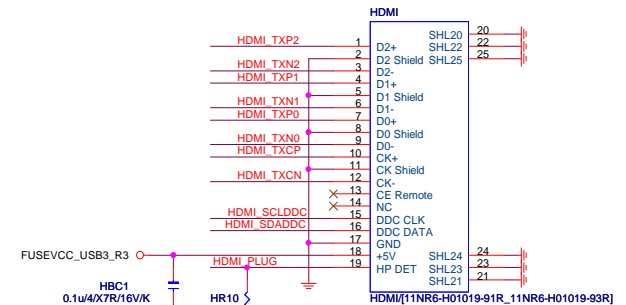
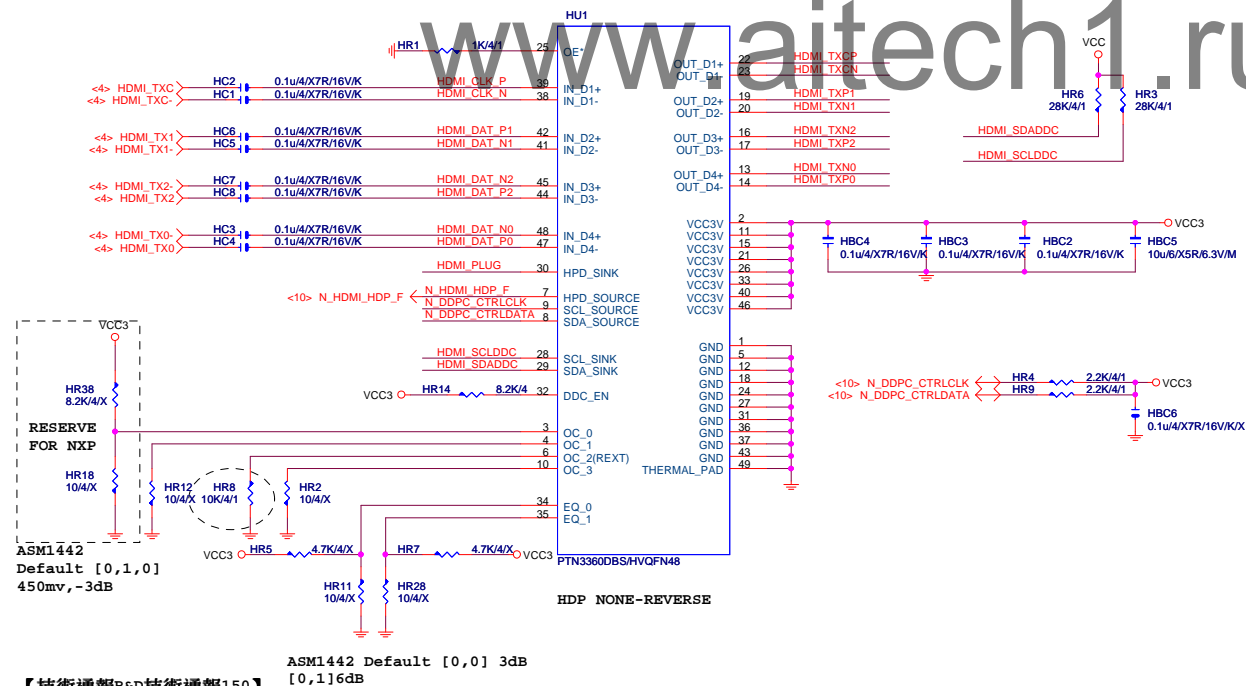
【技術通報R&D技術通報151】
33ohm Change to 68ohm



DVI LEVEL SHIFT



HDMI LEVEL SHIFT



【技術通報R&D技術通報150】

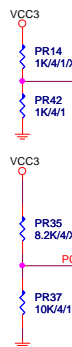
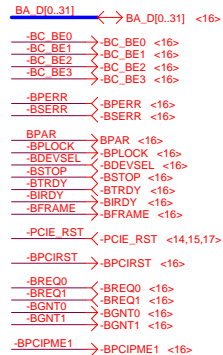
HDMI eye diagram1.4版(deep color)會fail

原因：因目前的HDMI訊號過長，造成RISING TIME過慢，而會壓到eye diagram

改善: ASMEDIA ASM1442 : 3.16K(PIN6 PULL DOWN電阻) 10ohm(PIN4 PULL DOWN電阻)

PCIE TO PCI

PCI:5/4/5 Impedance=50 +- 15%

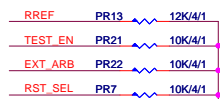
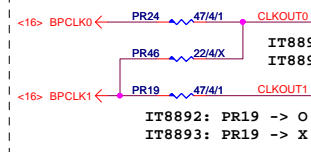


```
High: Enable PCI CLK 66MHz
Low: Disable PCI CLK 66MHz
```

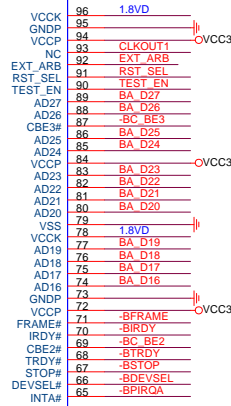
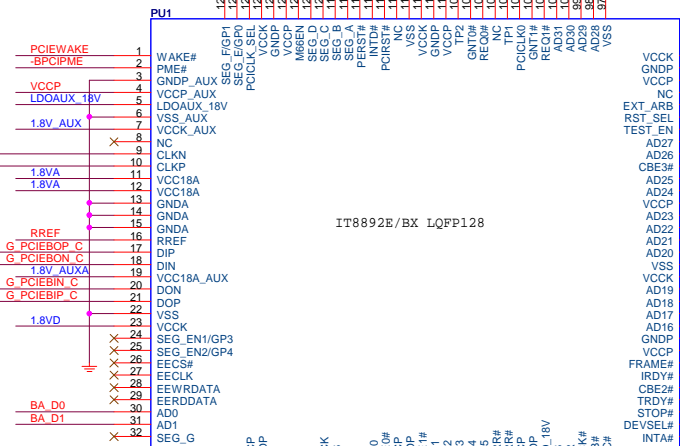
High: PCICLK INPUT form CLK Gen
Low: PCICLK OUTPUT form IT8893 chip

Co-Lay IT8893 (IT8893 CLKOUT1 N/A)

```
IT8892: PR24 -> 47ohm
IT8893: PR24 -> 22ohm
```

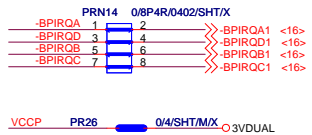


```
<10> G_-PBCLK >
<10> G PBCLK >
```



IT8892E/BX LQFP128

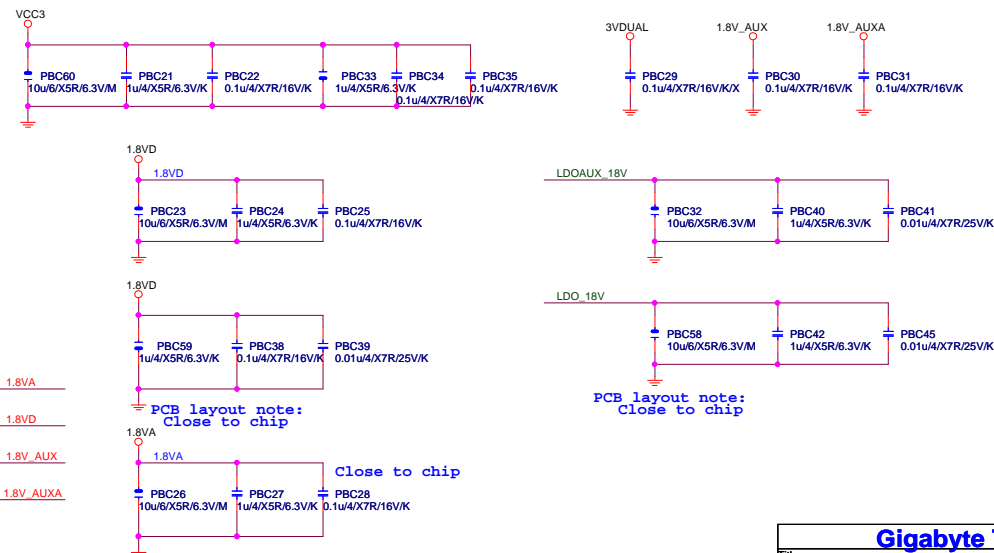
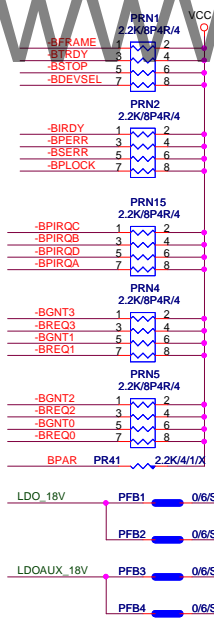
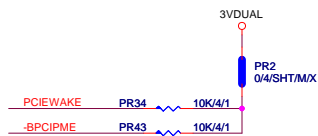
IT8892E/FX/S



PCI slot

PCI slot

```
-BPCIPME1 PR27 0/4/SHT/M/X >>>N_-PCIE_WAKE <12,14,15,24>
```



Close to chip

PCB layout note:
Close to chip

Gigabyte Technology

Title			
ITE IT8892E			
Size	Document Number	Rev	
Custom	GA-B85M-D3H	1.1	
Date:	Monday, July 15, 2013	Sheet	32 of 32